

# Topology Router

- The Intelligence of an Engineer
  - The Skill of a Designer
- The Speed of Auto-Routing

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Director, Market Development

**Mentor  
Graphics®**

# Challenges

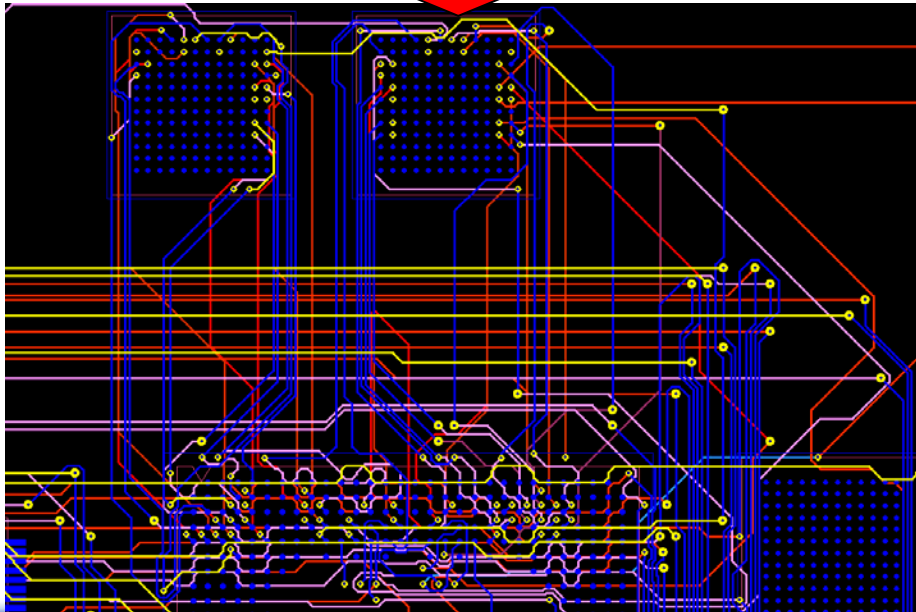
- **Reduction of design-cycle time for products that are typically designed manually**
- **Optimization of space and layers to produce competitive products**
  - Layer count = cost
  - Small form factor with highest functionality
- **Engineer to designer communication**



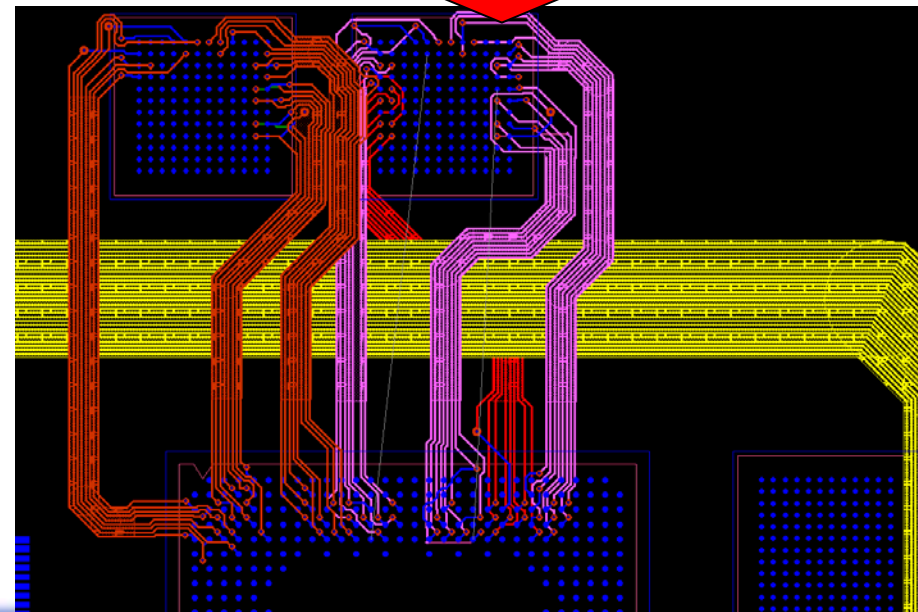
# Bus Routing

- **Auto-routers:**
  - Are much faster than manual routing
  - Produce electrically correct and manufacturable results
- **But:**
  - Manual routing can produce denser and higher quality results

**Auto-routers do this.  
They route one net at a time.**



**Designers do this.  
They recognize patterns and flows.**



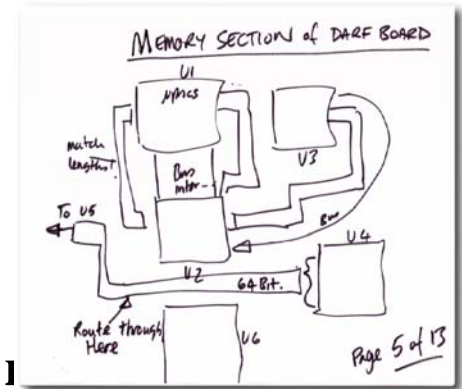


# Bus Routing

## Typical Design Process

### ■ Design engineer

- Typically sketches the physical bus systems and sub-systems architecture on paper
- Specific placement and bus interconnect guidelines
- Tries to determine if placement & estimated routing will meet delay requirements
- May have to give guidance “over board designer’s shoulder”



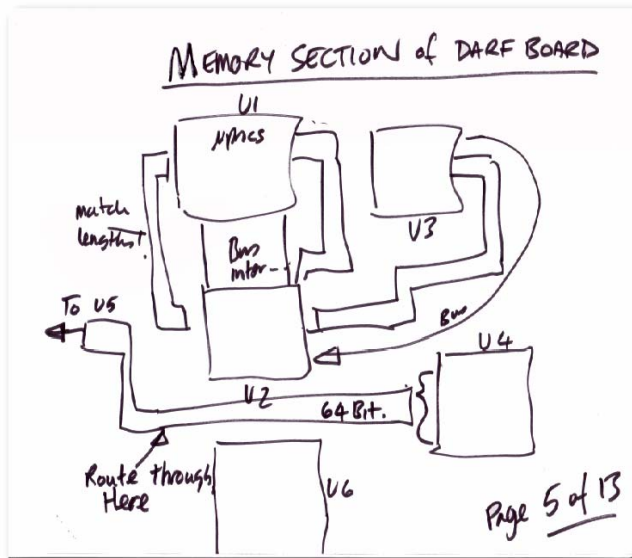
### ■ Board designer

- Looks for potential routing patterns and space that flow from component to component
- Plans ahead, knowing why a particular group of traces must route in a certain path on a specific layer (delay)

# Bus Routing

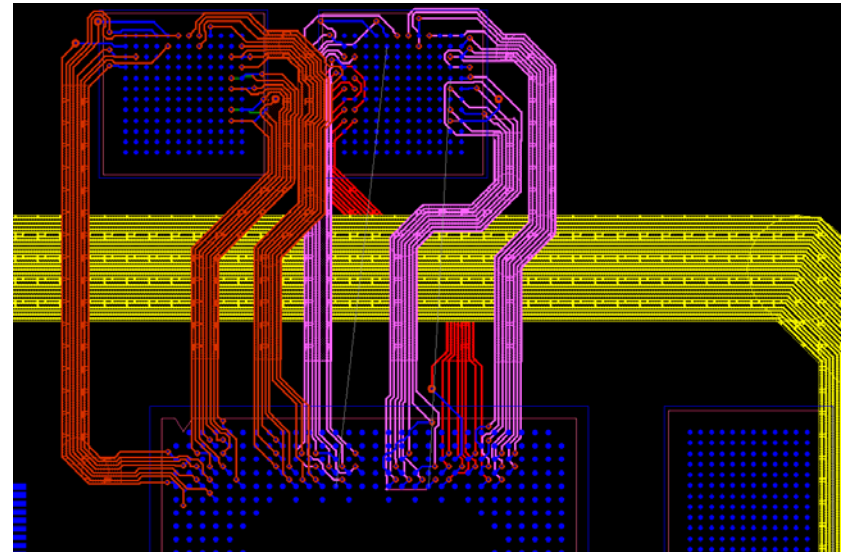
## Old methodology

### Paper Planning



**Engineer**

### Manual Routing



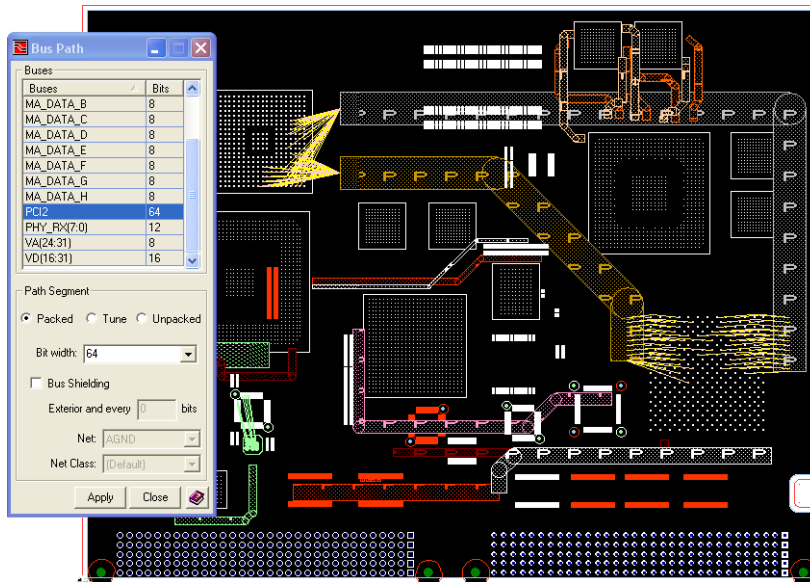
**Designer**

# Bus Routing

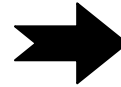
## *Topology-Driven Design with Engineer/Design Collaboration*

### New methodology

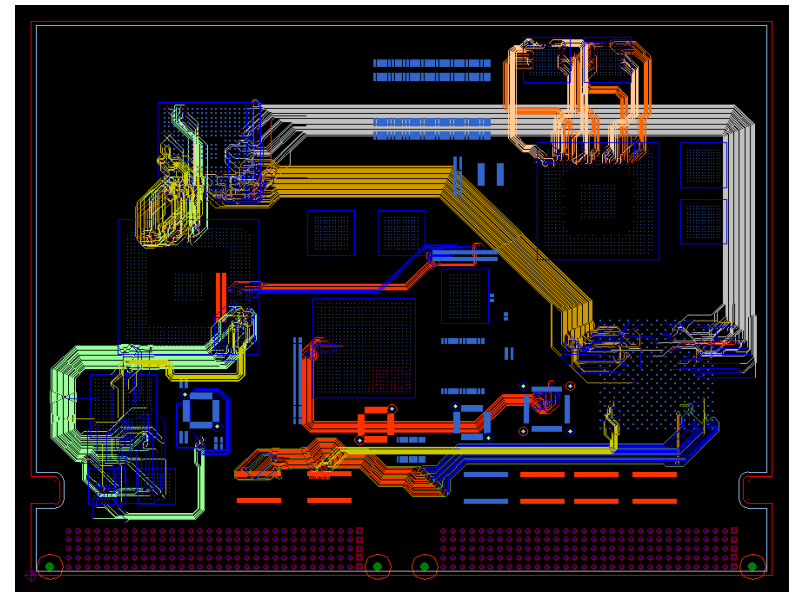
#### Topology Planner



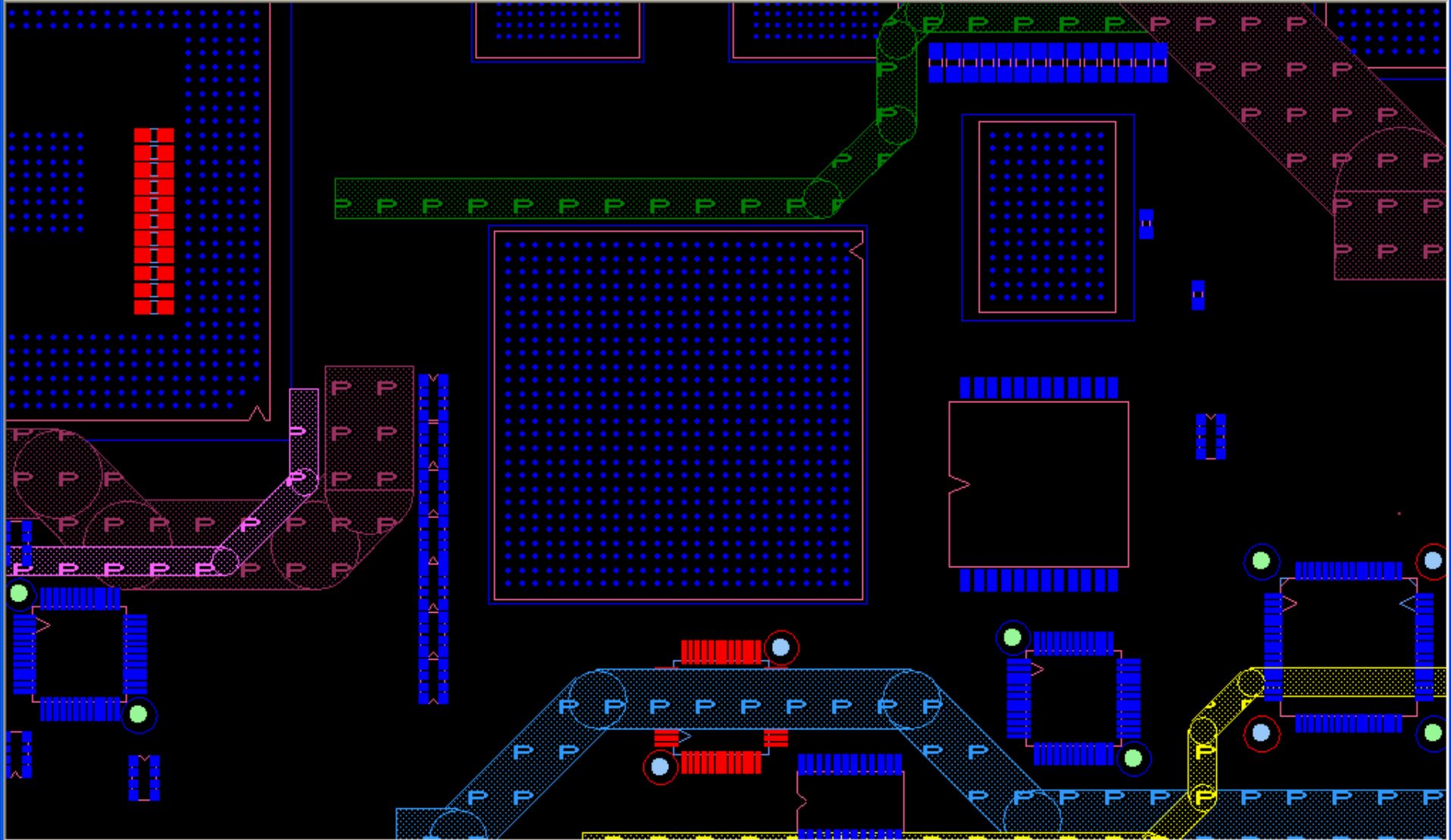
**Engineer Plan**

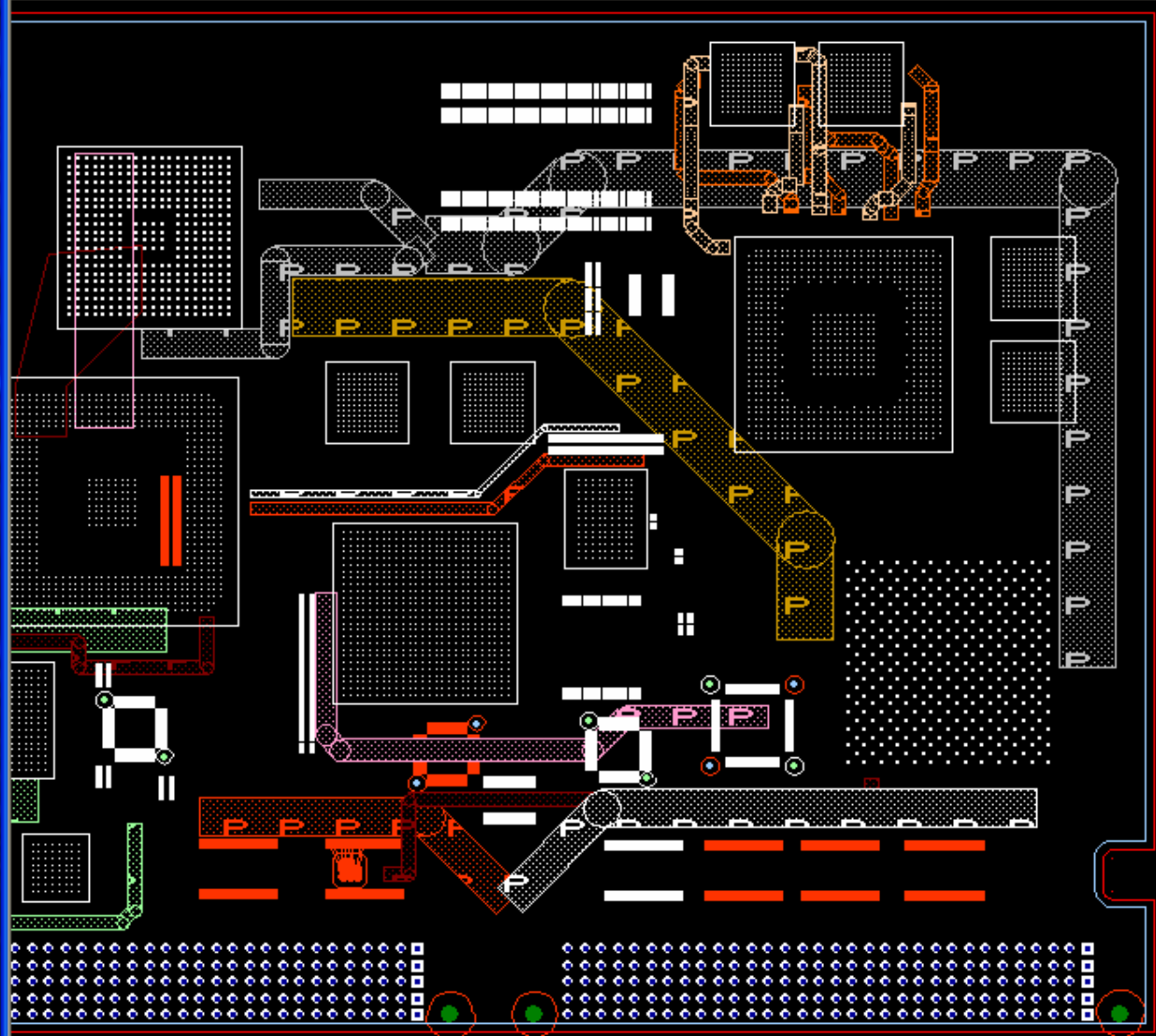


#### Topology Auto-Router

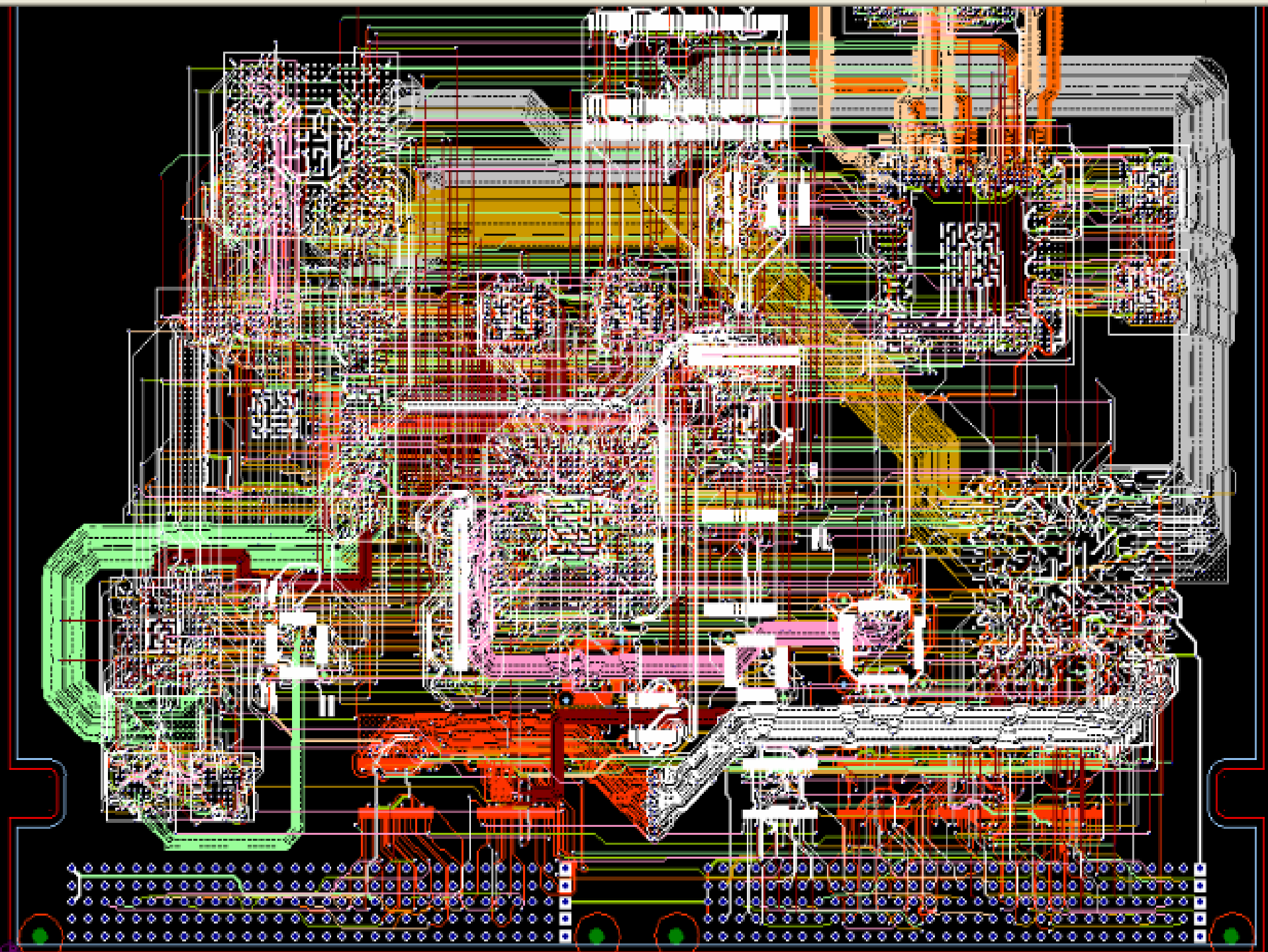


**Auto-Route Result**









# Special Routing Controls

## ■ Bus with shielding

The image shows two dialog boxes from a PCB design tool. The top dialog is 'Auto Route' and the bottom is 'Bus Path'.

**Auto Route Dialog:**

Pass definition: Effort

Pass	Pass Type	Items to Route	Order	Start	End	Now	Layers	Via Grid	Rte. Grid	Fix	Pause
<input type="checkbox"/>	Straight Line Interconn...	All Nets	Auto	1	3		All Enabled	(Default)	(Default)	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	Bus Route	Buses with Paths...	Auto	1	1		All Enabled	(Default)	(Default)	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/>	Bus Shielding	All Nets	Auto	1	1		All Enabled	(Default)	(Default)	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	Tune Delay	Tuned Nets	Auto	1	1		All Enabled	(Default)	(Default)	<input type="checkbox"/>	<input type="checkbox"/>

Options:

- Route during Fanout (for microvias)
- Save design before starting Route
- Allow "Cleanup" if not routed 100%

AutoSave interval: 60 (min)

	Considered	Attempted	# Routed	To Try	Opens	% Routed	Vias	CPU (h:m:s)	CLK (h:m:s)
Effort:	662	0	0	662	662	0.00	0	00:00:02	00:00:02
Total:	.....	.....	.....	.....	2923	2.15	33	00:00:14	00:00:14

Scheme: Local\_bus\_route

Buttons: XtremeAR, Route, Close

**Bus Path Dialog:**

Buses:

Buses	Bits
MA_DATA_B	8
MA_DATA_C	8
MA_DATA_D	8
MA_DATA_E	8
MA_DATA_F	8
MA_DATA_G	8
MA_DATA_H	8
PCI2	64
PHY_RX(7:0)	12
VA(24:31)	8
VDI(16:31)	16

Path Segment:

Packed  Tune  Unpacked

Bit width: 16

Bus Shielding

Exterior and every 4 bits

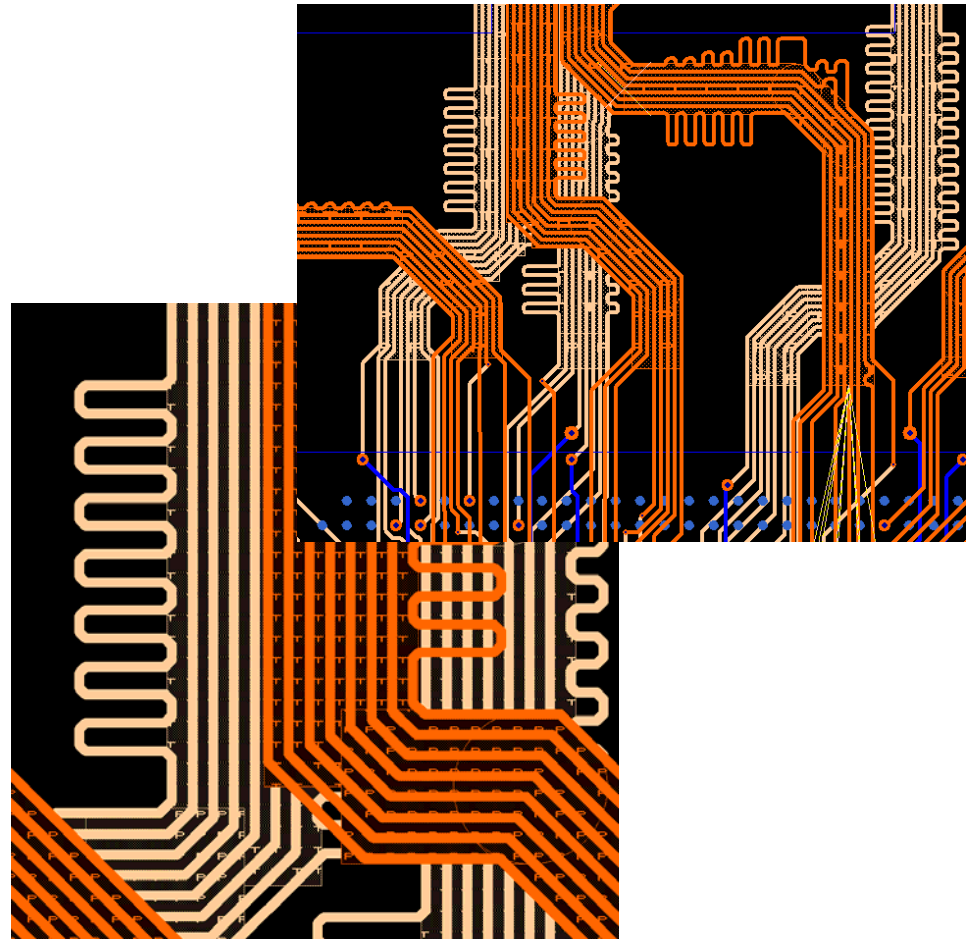
Net: AGND

Net Class: (Default)

Buttons: Apply, Close

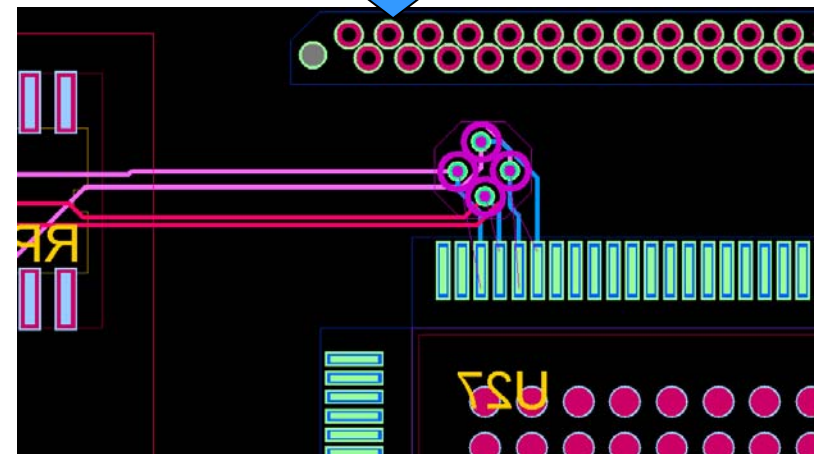
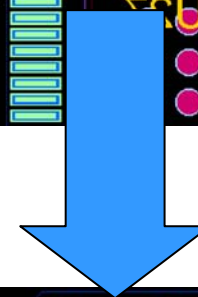
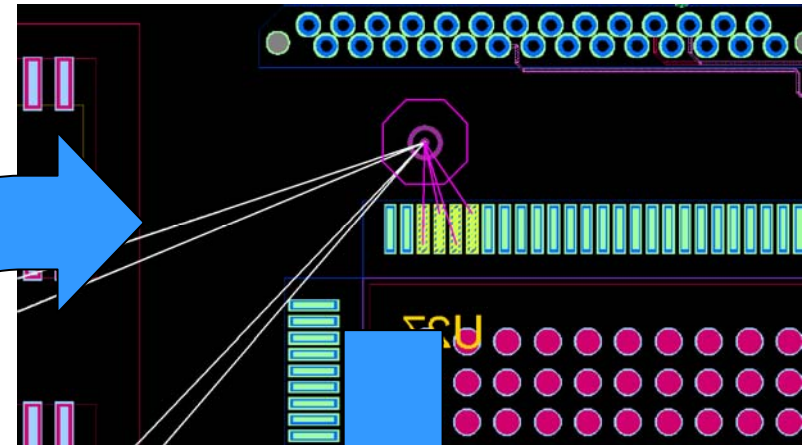
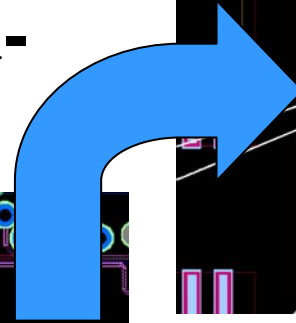
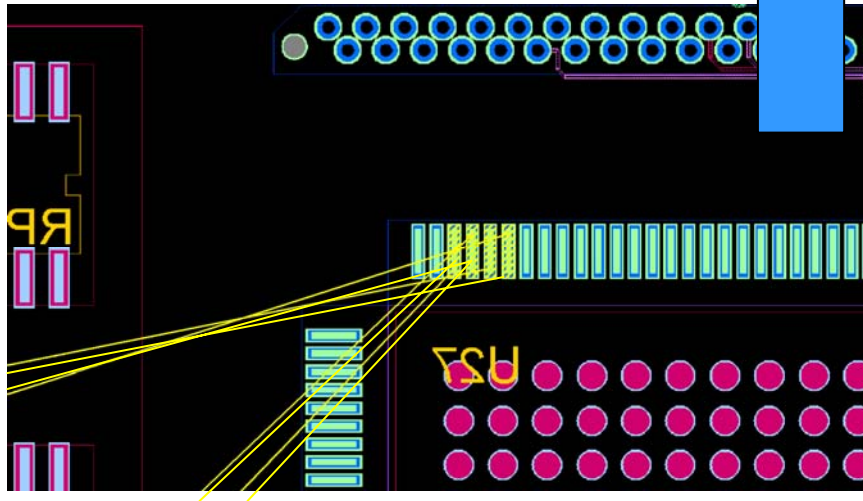
# Special Routing Controls

- Designated high-speed tuning areas



# Special Routing Controls

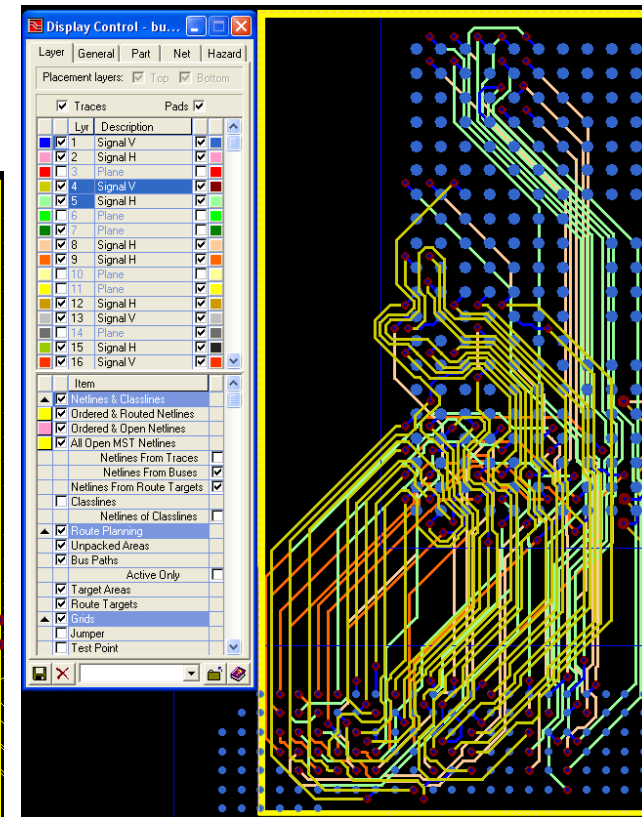
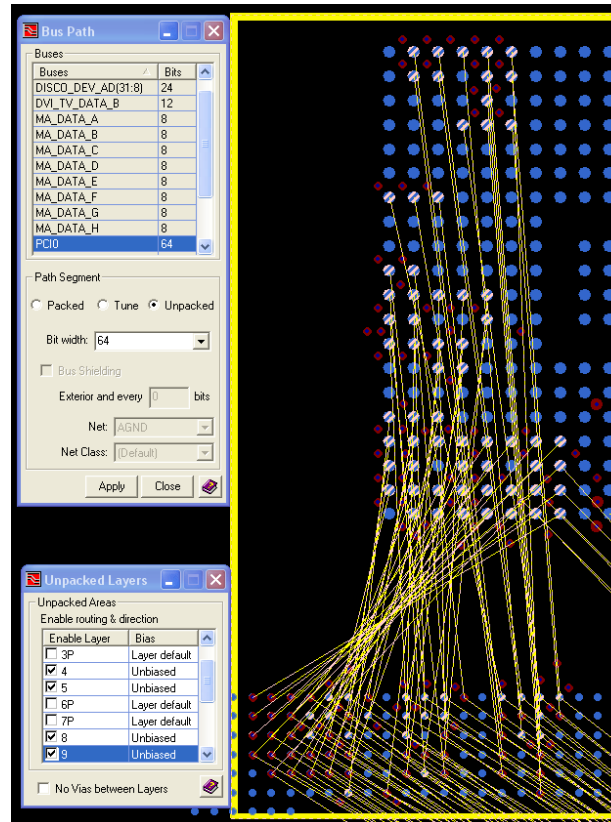
- Target areas for non-bus routing control





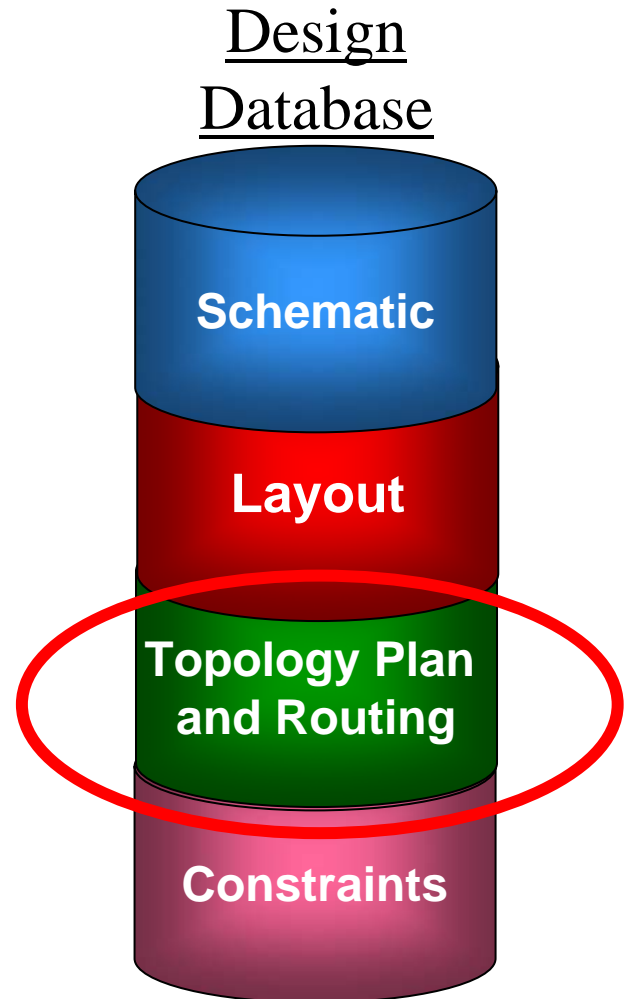
# Special Routing Controls

## ■ Routing bias control areas



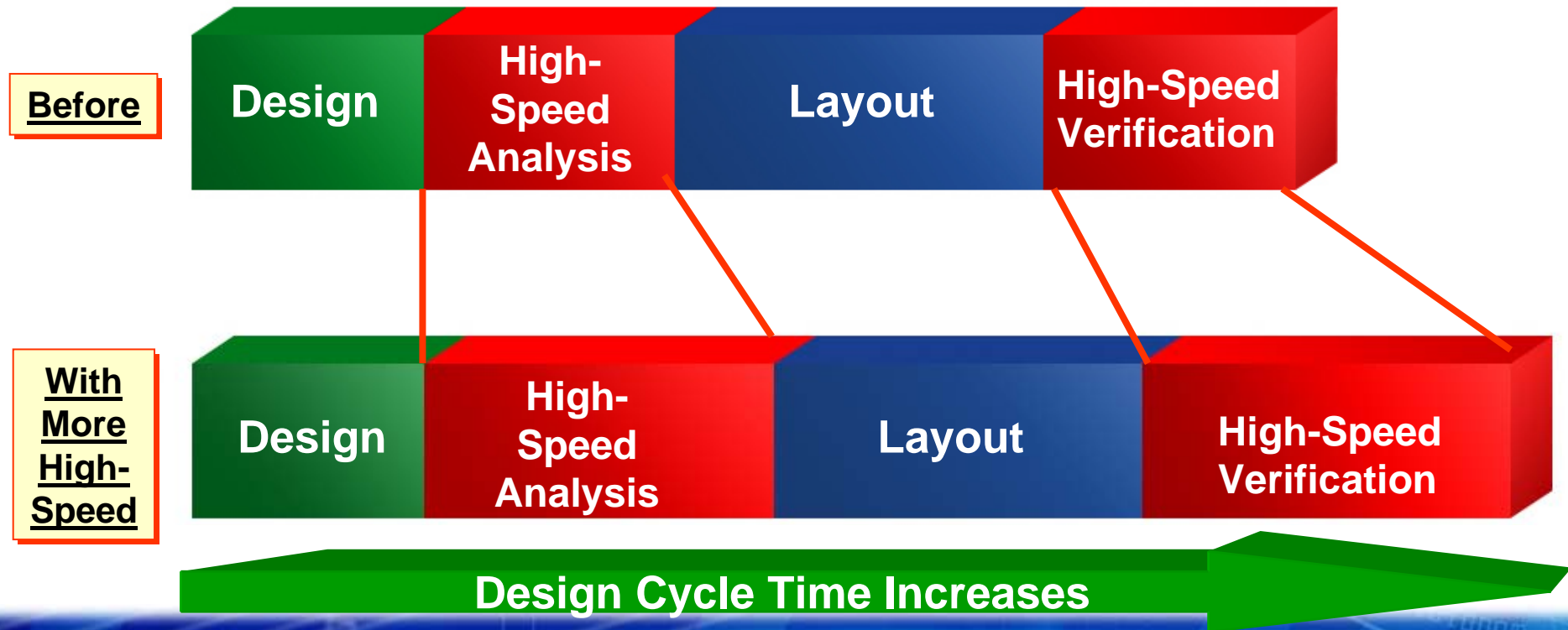
# Design Iterations and Reuse

- **Topology plan and routing becomes part of design database**
  - Design team can iterate to best solution without re-entry – **performance and cost optimization**
  - ECOs are easily implemented – **reduced design cycle time**
  - Database can be re-used in future products, “design reuse” – **productivity and quality**



# Japanese Computer Supplier, Challenge

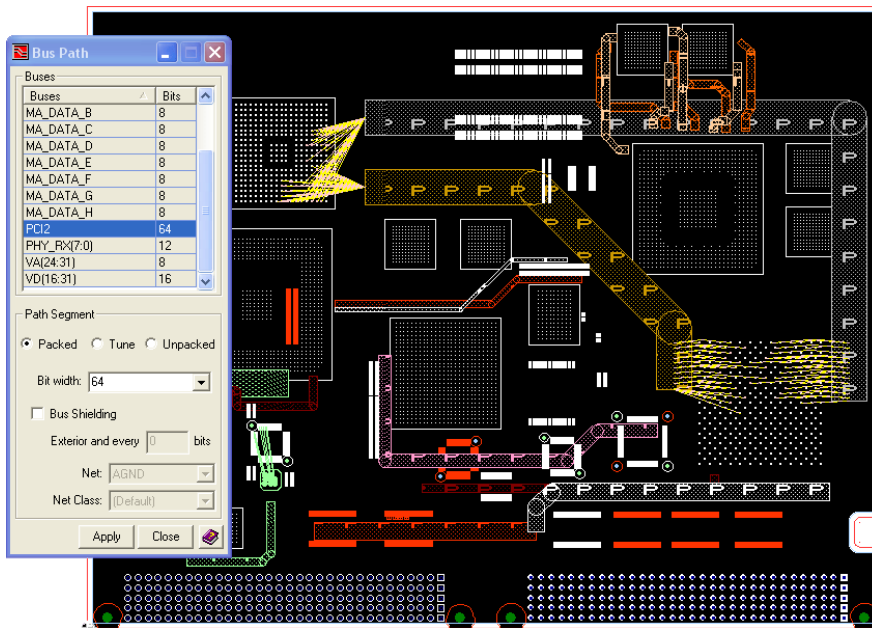
- Increase in high-speed nets is requiring more time in analysis and verification
- Result: Trend to longer design cycle time, missing time-to-market windows



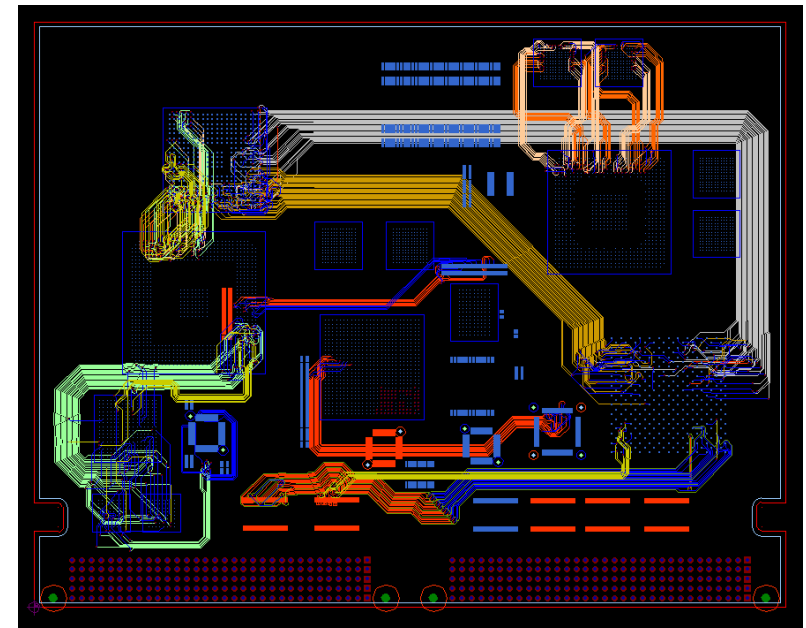
# Solution Approach

## Reduce manual layout time by 50%

- Worked with Mentor to develop “Topology Router”
- Mimics expertise of CAD designer with speed of auto-router



Engineer Plan



Auto-Route Result



# Results with Topology Router

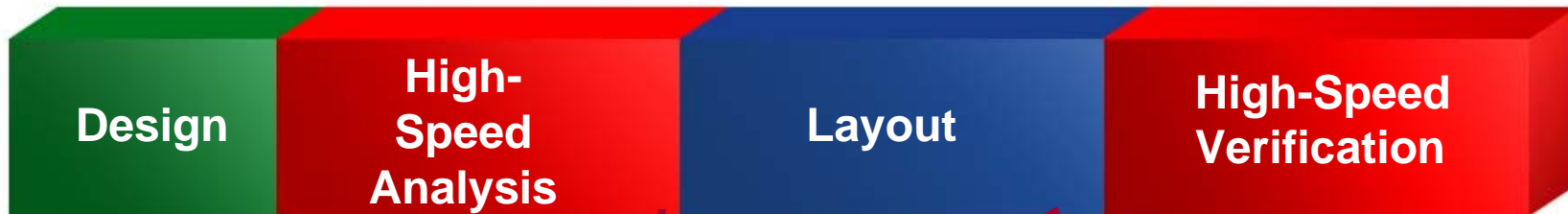
- “With the Topology Router technology, we will reduce our layout time by at least 50%, allowing more time for high-speed verification, and still meet our time-to-market schedules.”

- Japanese computer supplier

Before



With  
More  
High-  
Speed



With  
Topology  
Router



Reduction

# Benefits of Topology Router

- Reduced product design cycle time – capitalize on auto-routing speed
- More compact designs – mimics the expertise of an experienced designer
  - More functionality in smaller spaces
- Higher quality designs
  - Manufacturability
  - Performance
- Efficient re-use of design databases in future products
- Engineer to designer communication – no more paper or over the shoulder!



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