Calibre LFD (Litho-Friendly Design)

Capturing Process Variations to Improve Design Robustness

Product Launch - Editor Presentation

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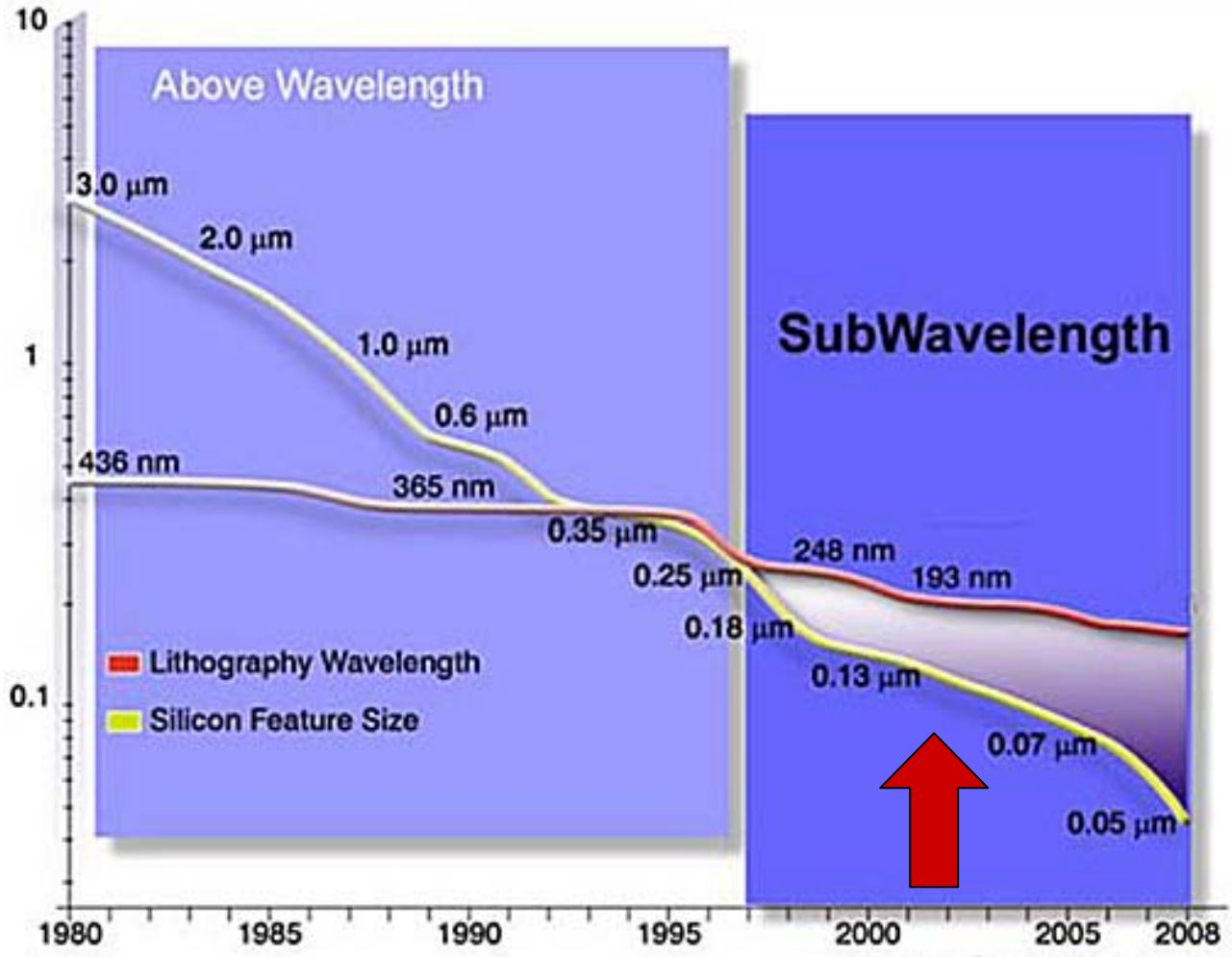
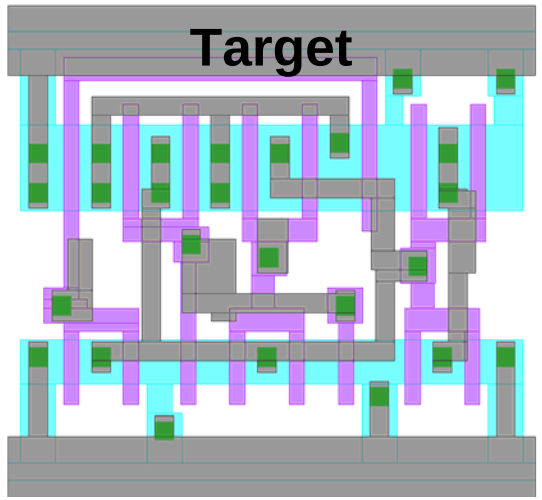
VP AND GENERAL MANAGER
DESIGN TO SILICON DIVISION

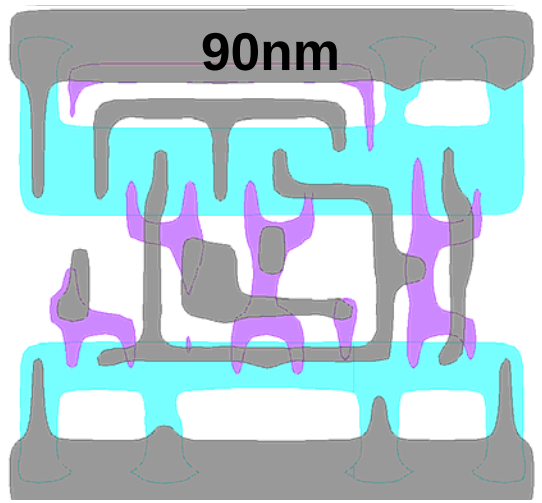
Mentor Graphics®

Q1 2006

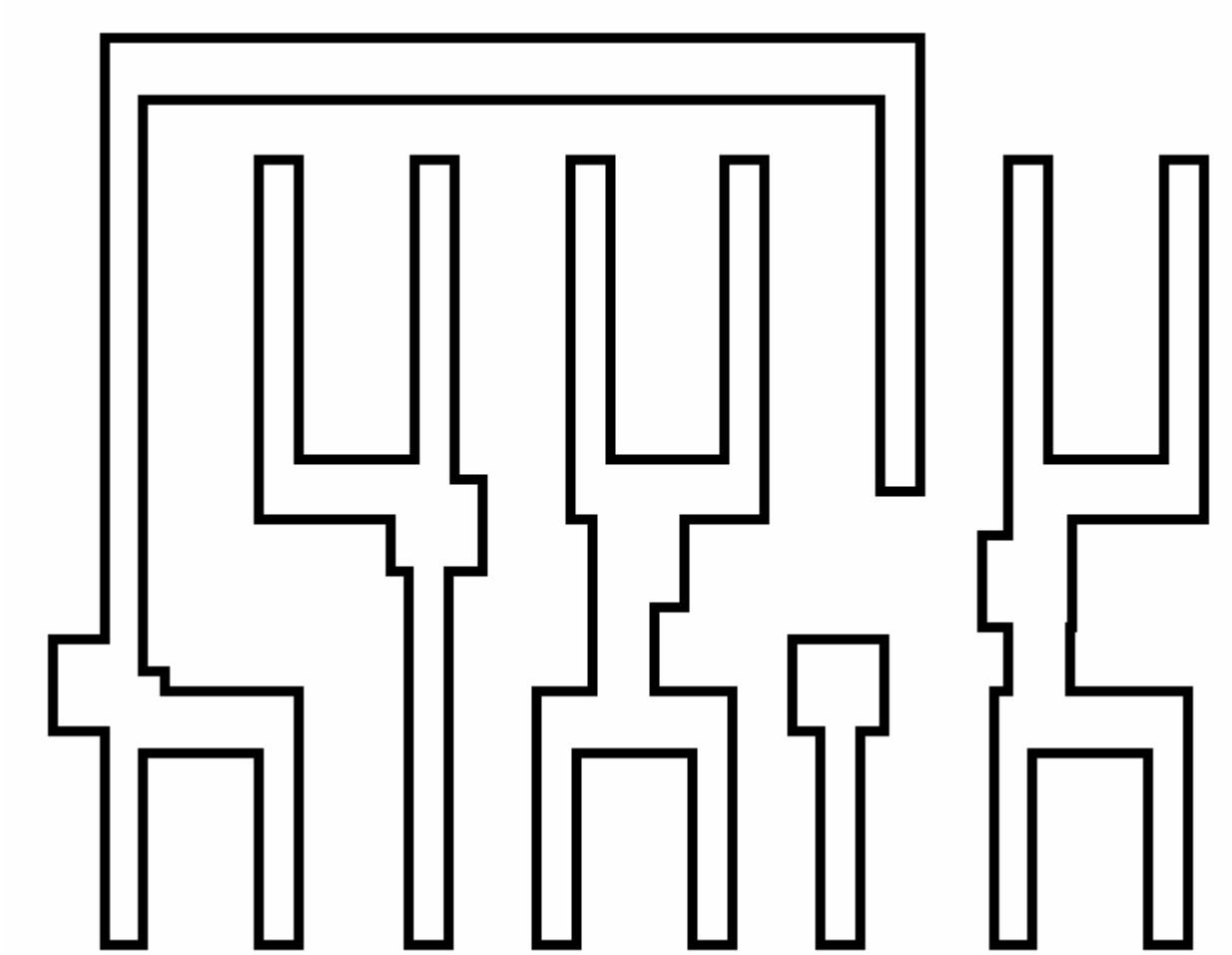
Without EDA and OPC, There Would Be No Advanced Node



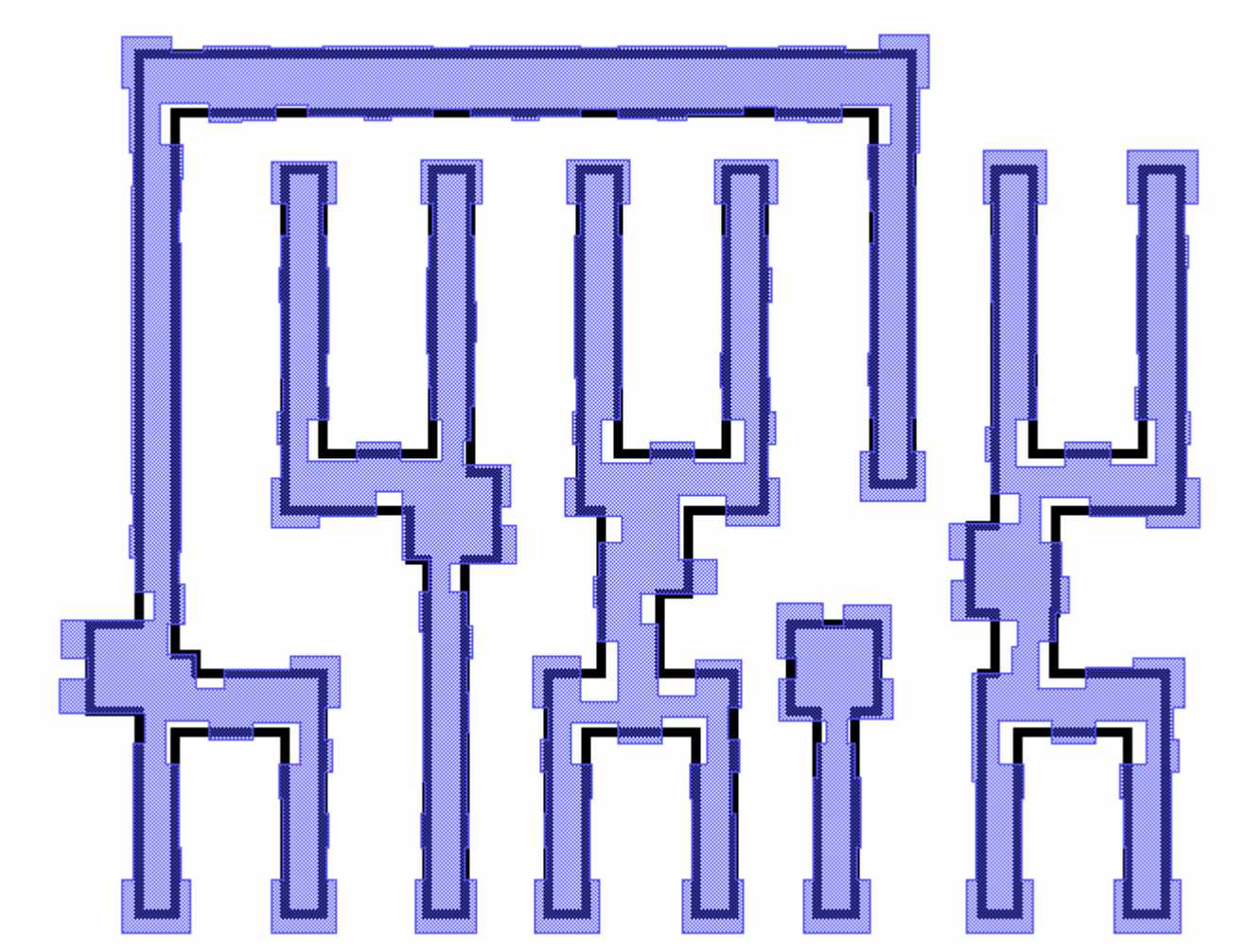




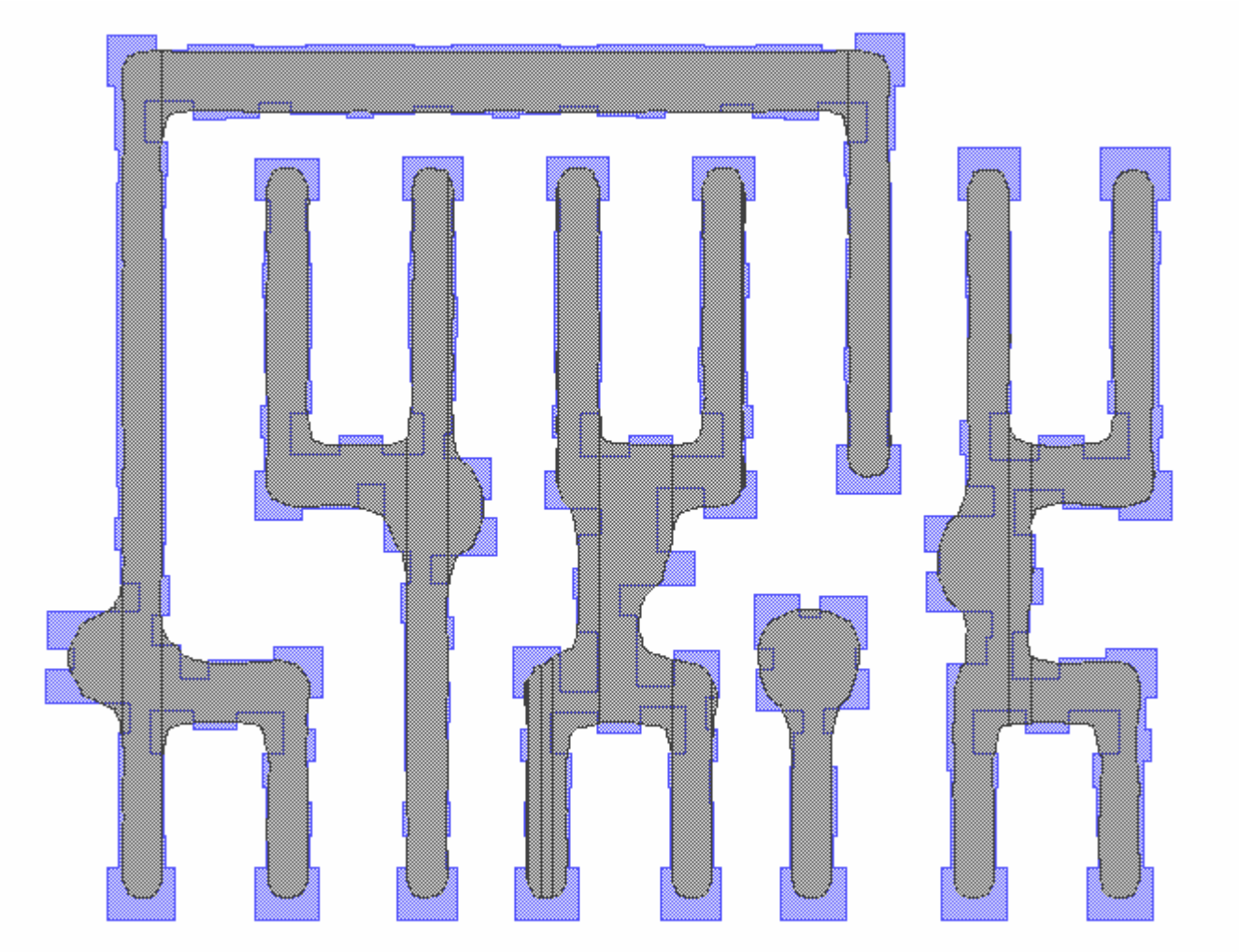
Target: 90nm



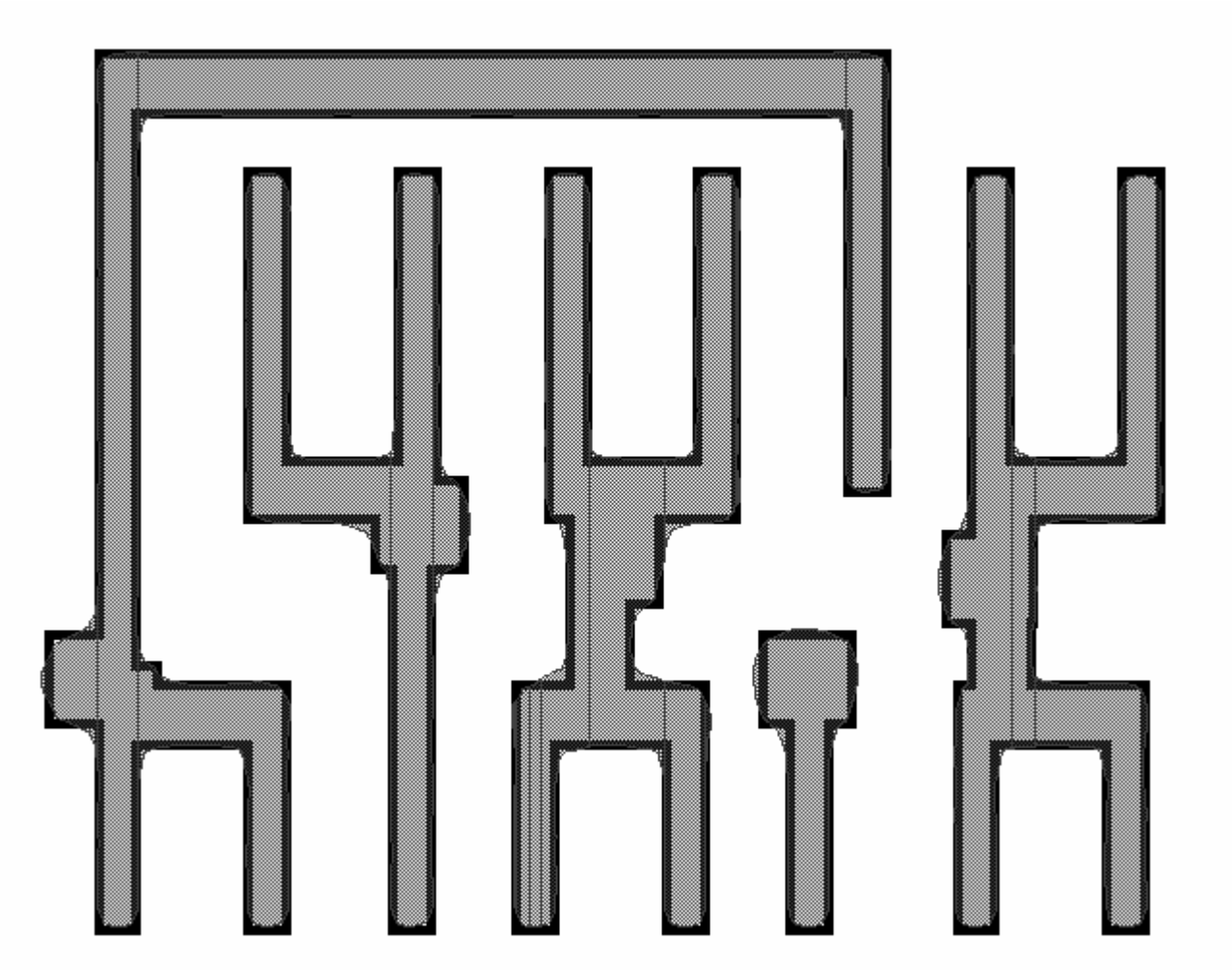
90nm Poly OPC



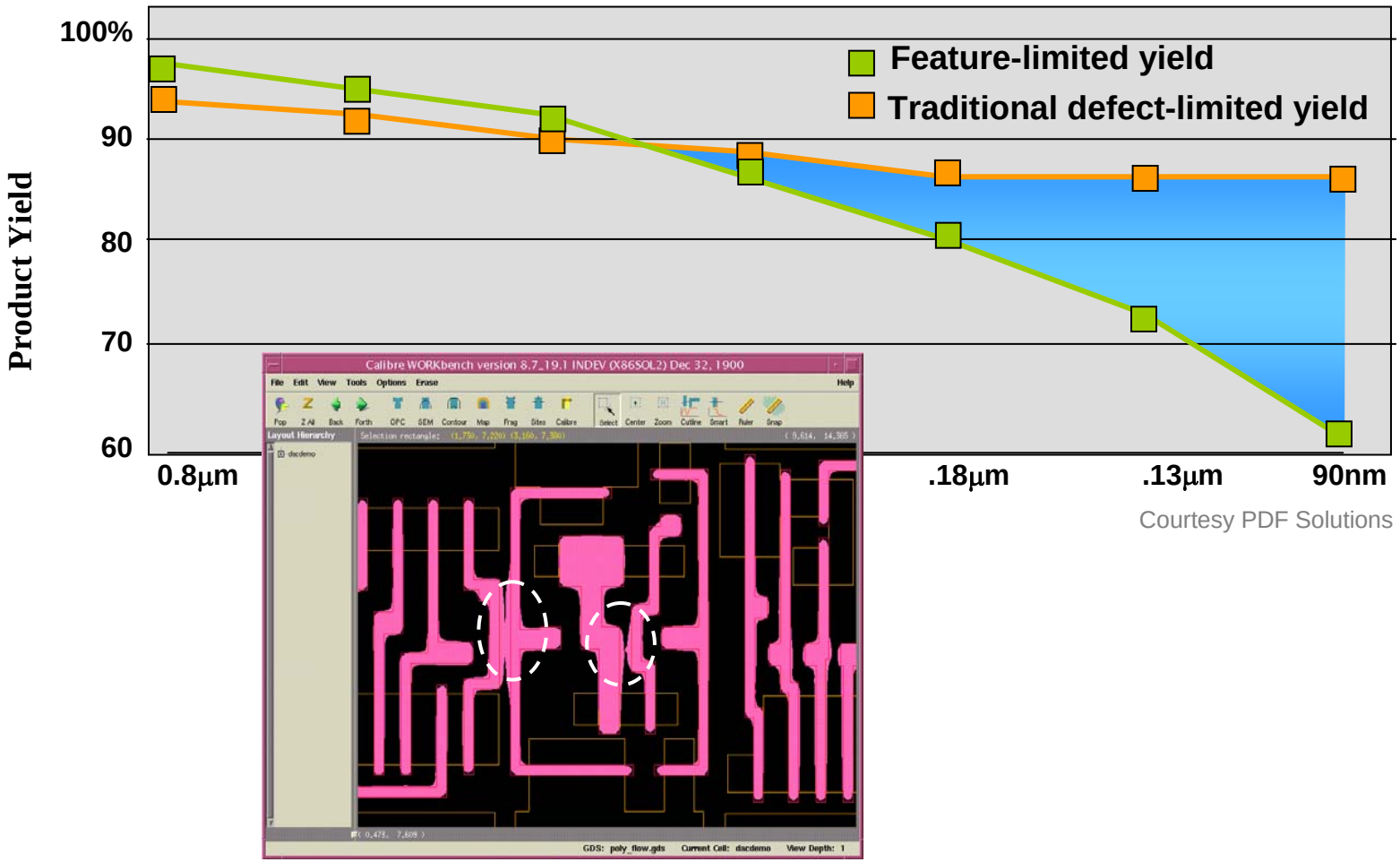
90nm Poly with OPC



Silicon and Target

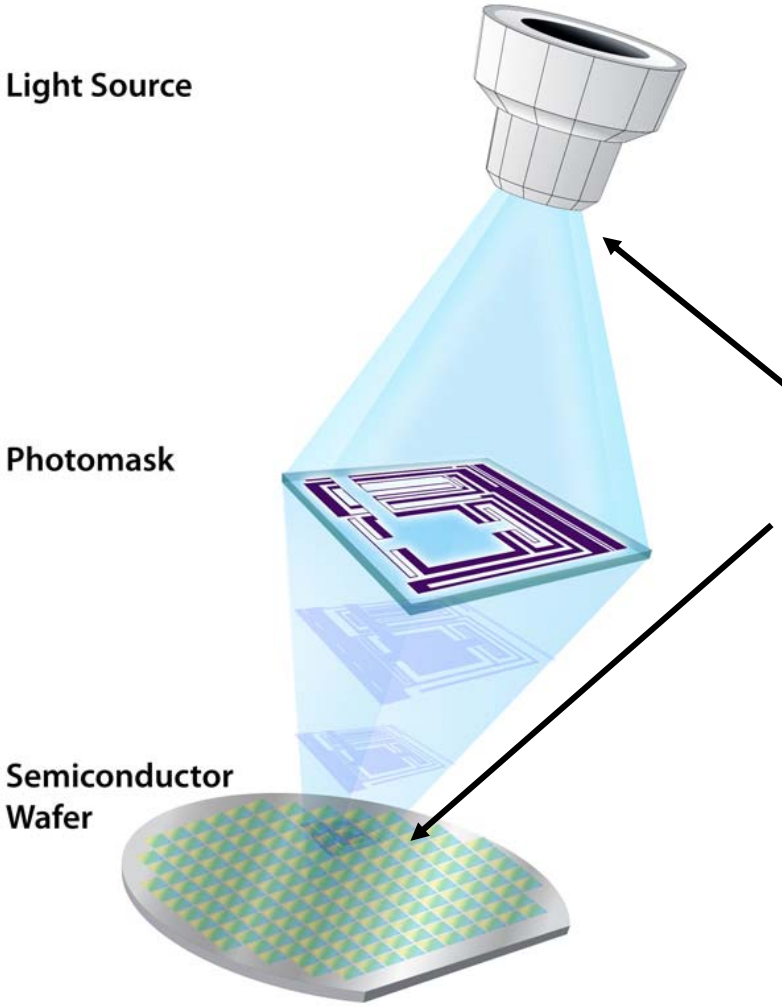


Yield Management Moves Into Design



Courtesy PDF Solutions

Sources of Lithographic Variability



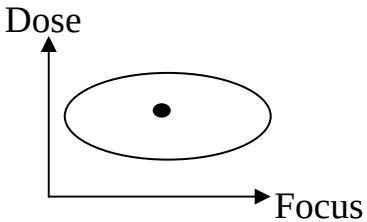
Two main sources of lithographic variability

- **Dose: variation in intensity**
- **Focus: variation of wafer in z axis**

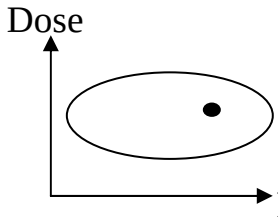
Defines a manufacturing window, commonly referred to as

“the process window”

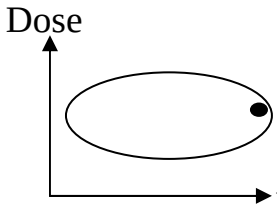
Litho Variation and Yield



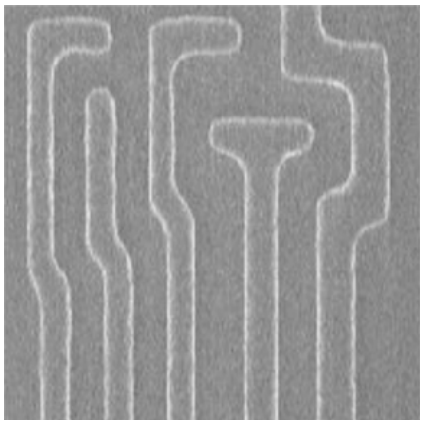
Best Focus



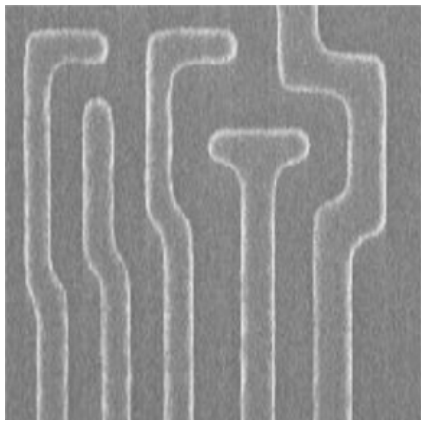
+100nm Defocus



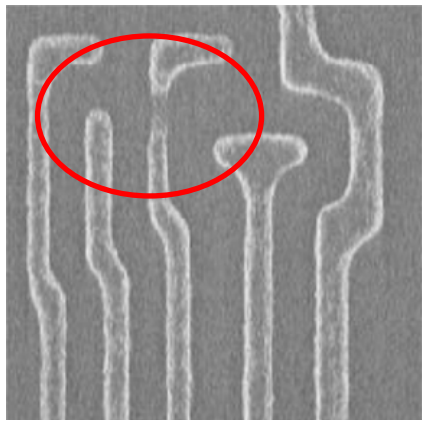
+200nm Defocus



DRC Clean



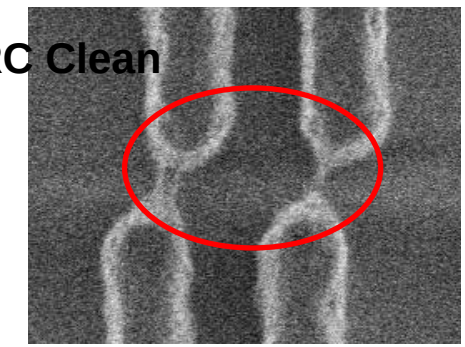
DRC Clean



pinching

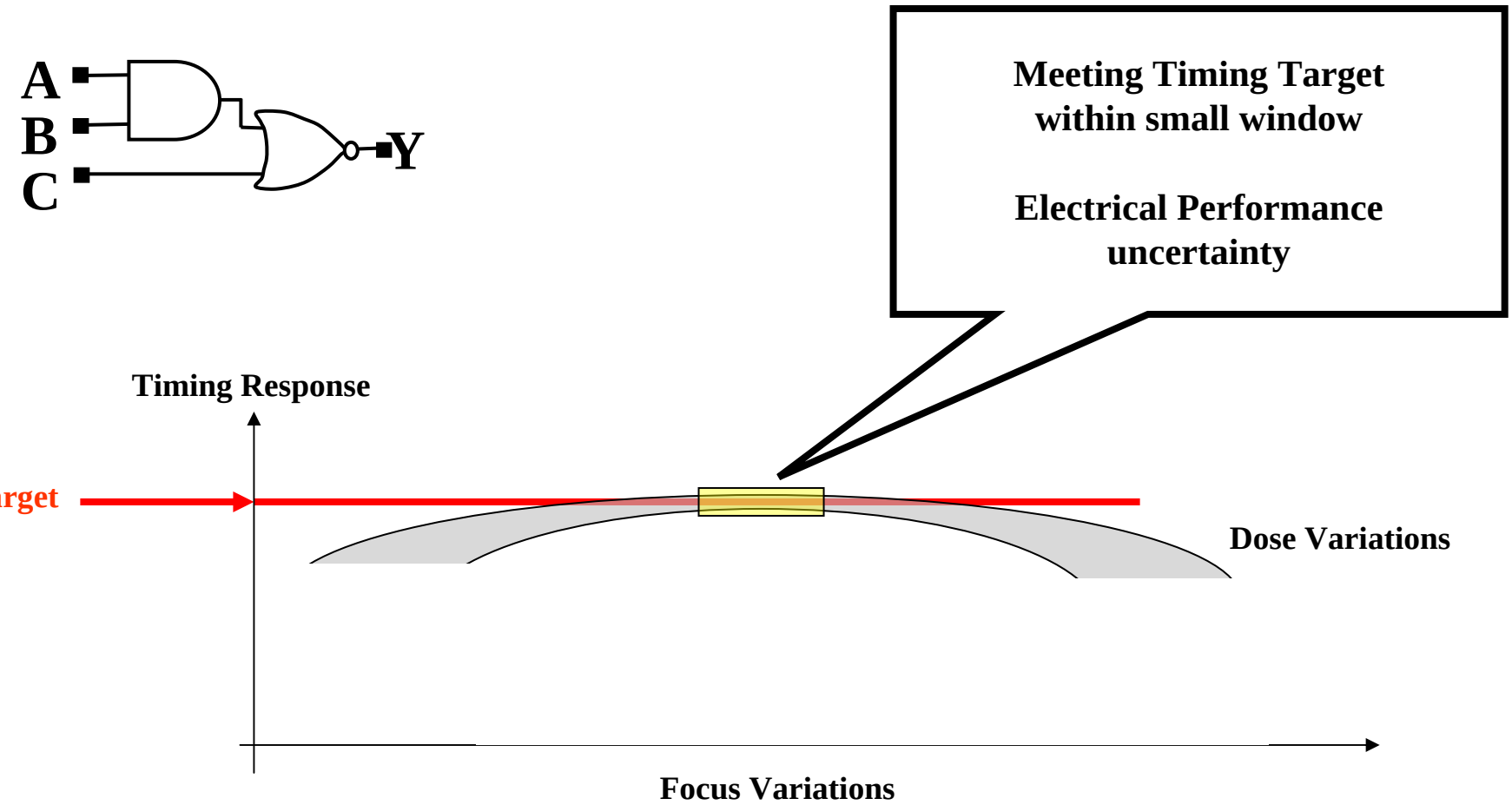
DRC Clean

bridging

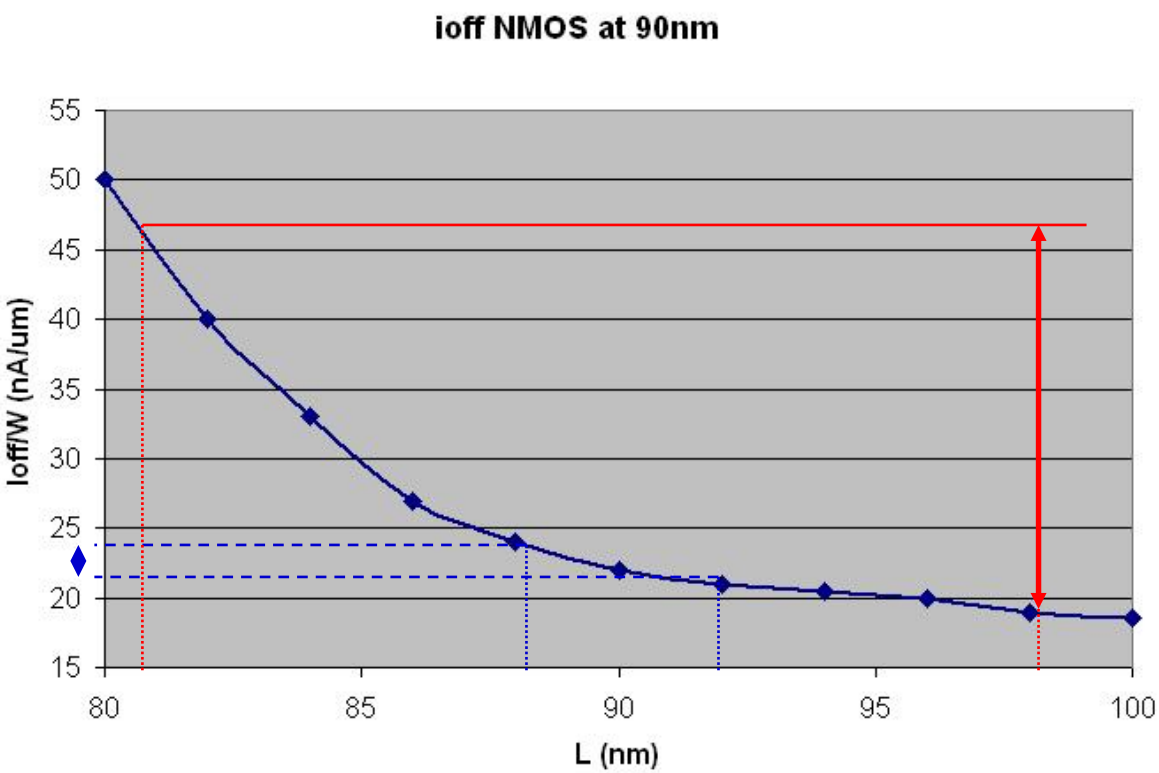


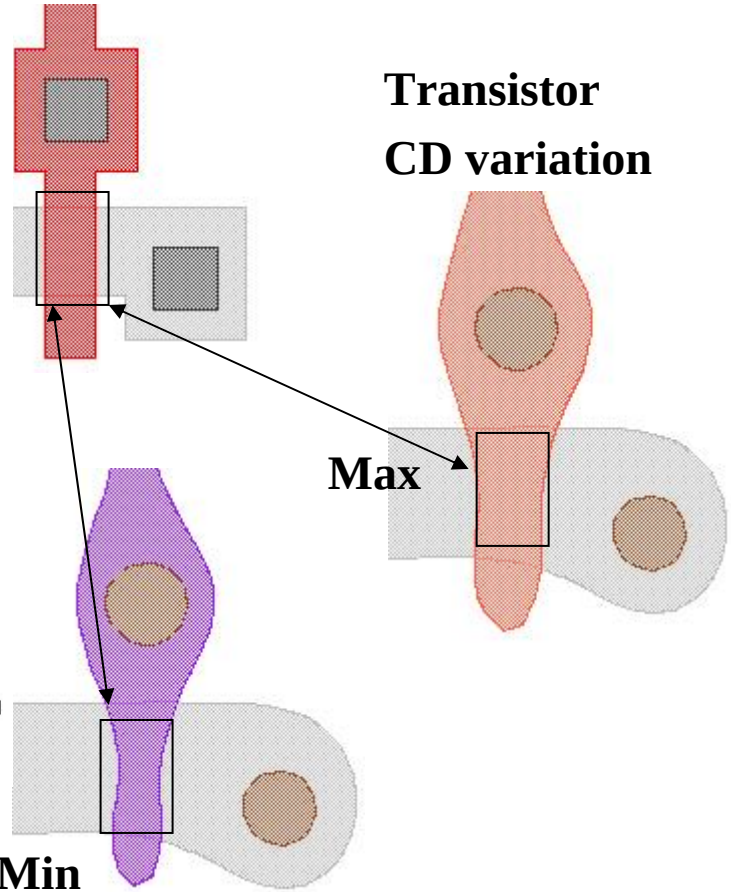
At ≤ 90nm technologies, certain layout topologies fail across process windows

Electrical Variability with Process Windows



Power/Leakage Variability



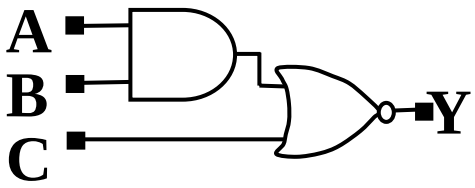


At 90nm

CD variation of 20%

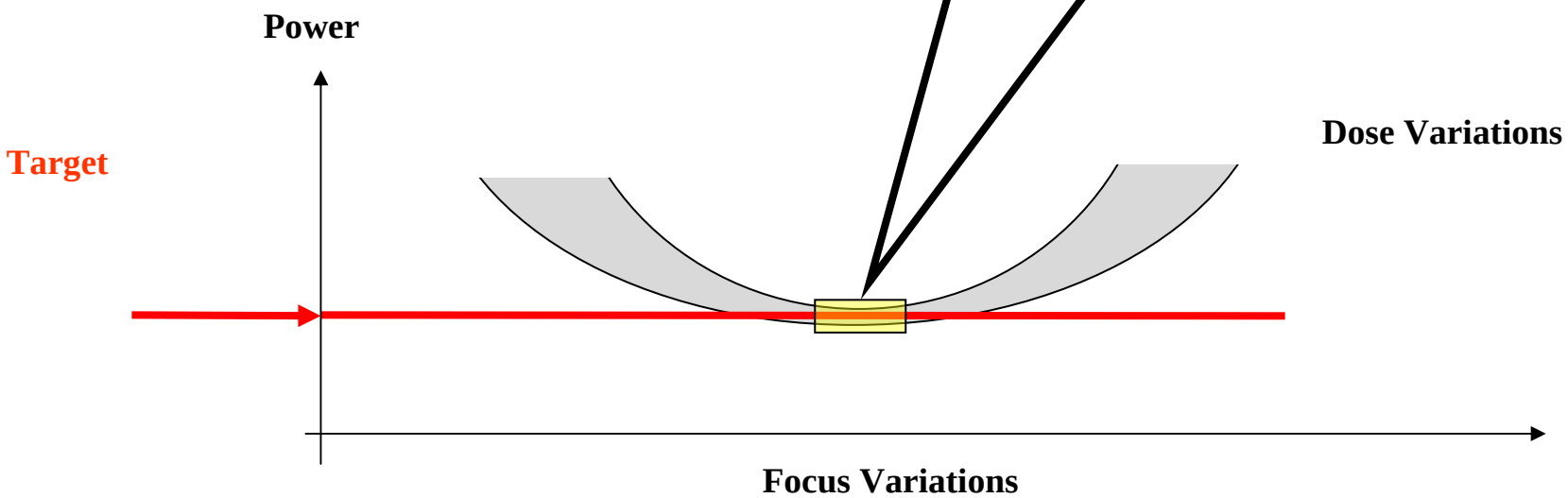
Results ~2x Ioff variation

Electrical Variability with Process Windows



Meeting Power Target
within small window

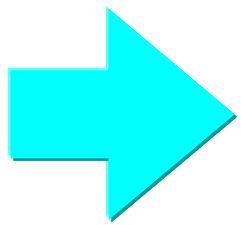
Electrical Performance
uncertainty



Solution to Lithographic Variability Issues

- **Because of**
  - **Layout failure and sensitivity across process windows**
  - **Electrical performance uncertainty across process windows**
  - **Power/leakage variability**

Solution is to manage the impact of process variations during design stage to improve layout robustness



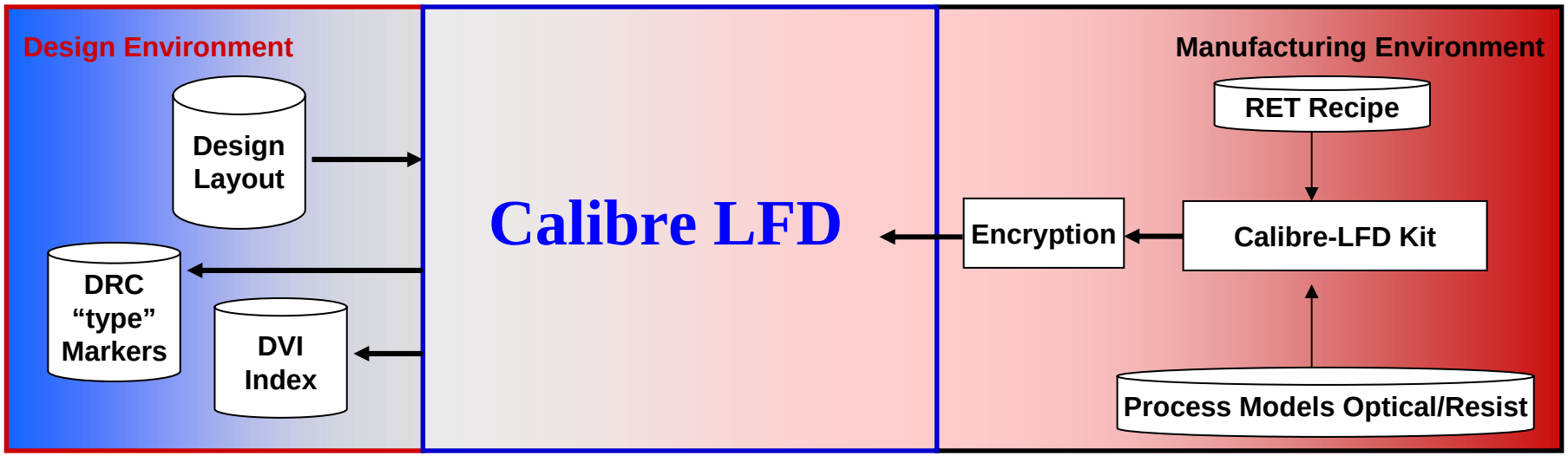
Litho-Friendly Design Technology

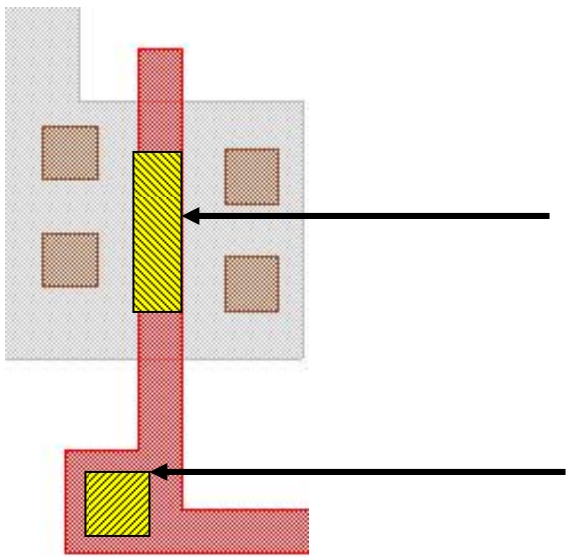
Introducing Calibre LFD

- **Calibre LFD is a new tool that provides significant benefits to the *Layout Designer* by:**
  - **Checking lithographic variation and failure during the design stage**
  - **Taking physical verification to the next level**
    - **From rule based only**
    - **To rule and model based**

- **Based on Mentor's technology leadership with Calibre DRC and Calibre OPC, we are ideally positioned to bridge the DFM divide between design and manufacturing**

Calibre LFD Technology





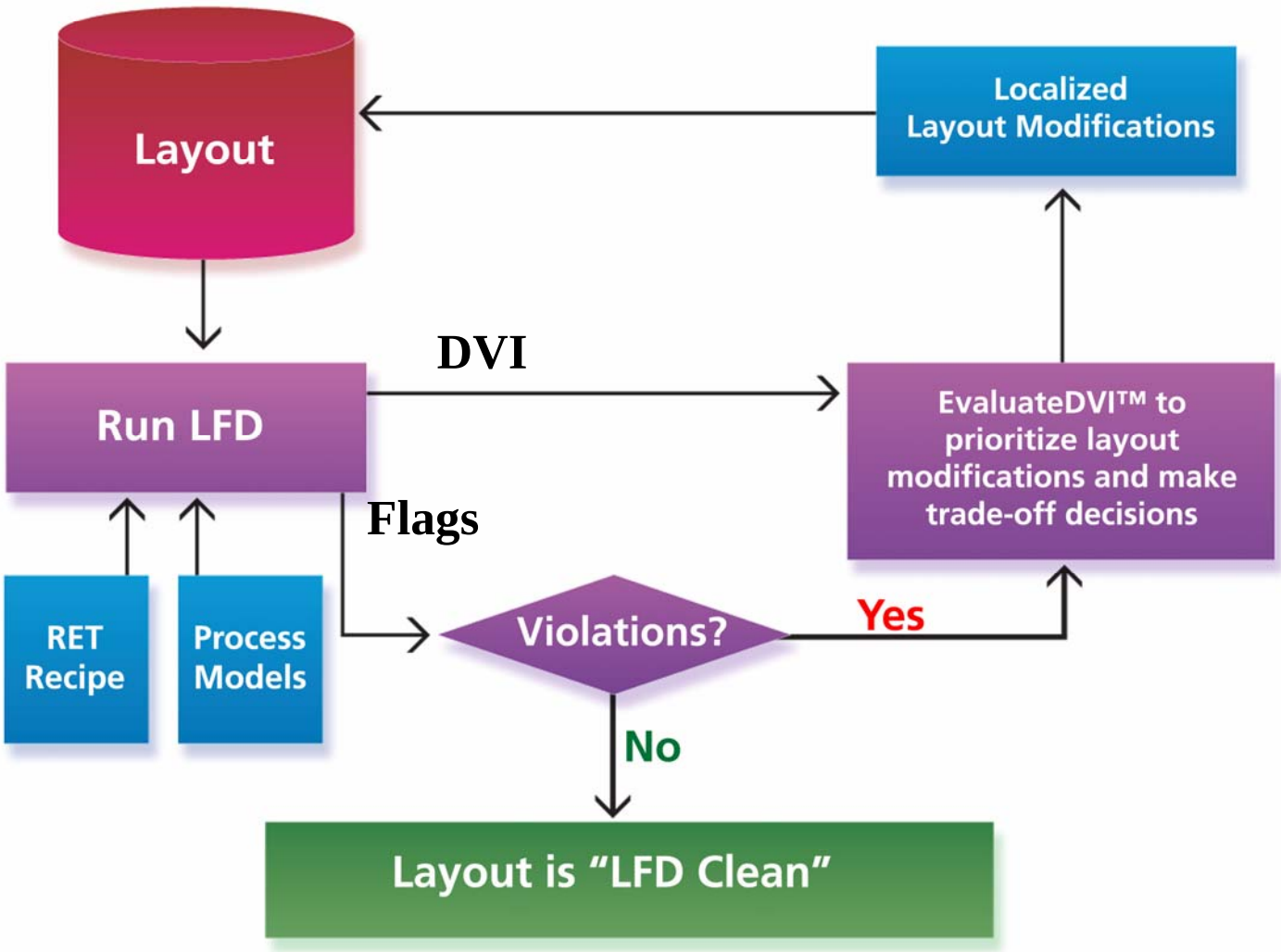
Poly:
Too narrow

Contact:
Too small

Layer	DVI
POLY	0.25
CONTACT	0.40

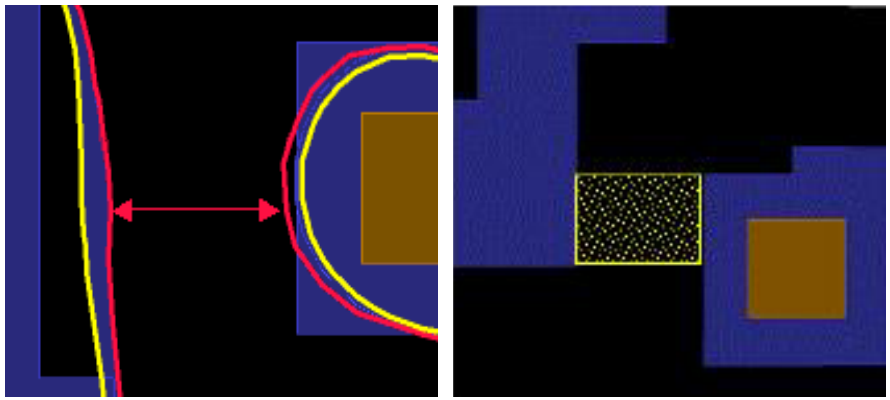
DVI™:
Design Variability Index
Helps designers identify sensitive topologies

Adding LFD Step to Design Creation Flow

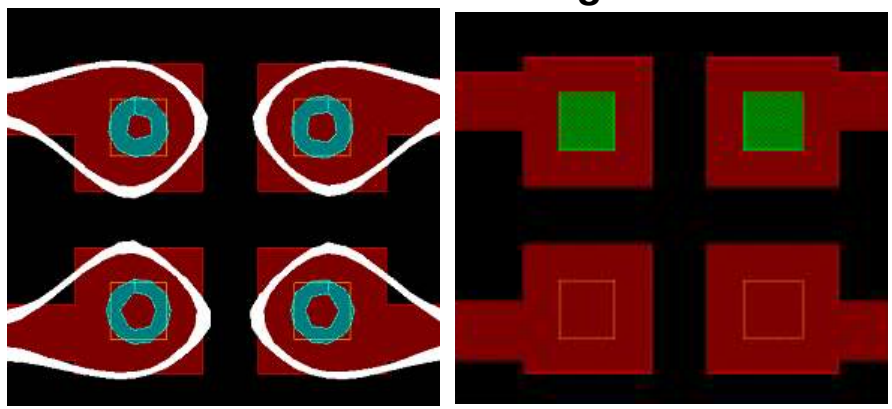


Moving to Model-Based Design Rule Checking

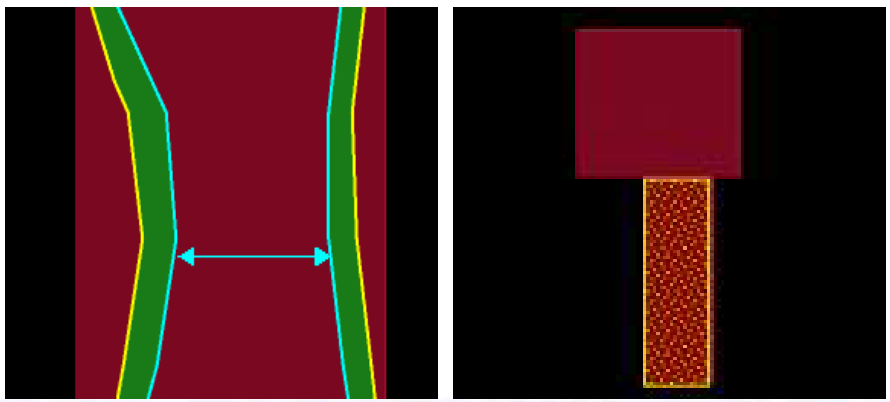
Minimum Space Check (MSC)- Bridging



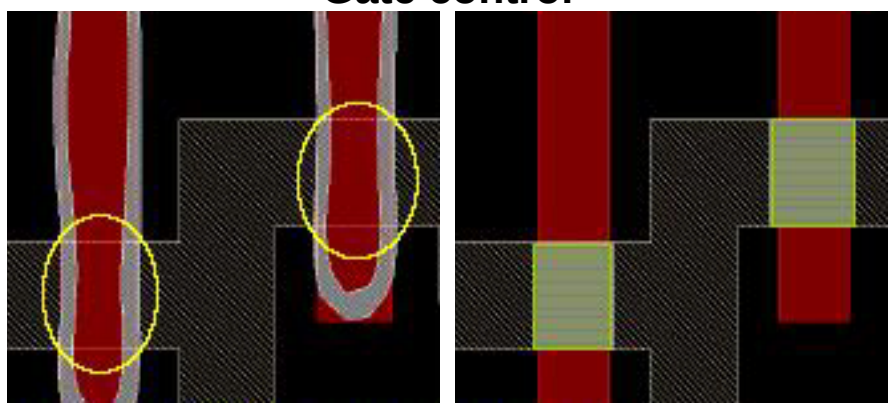
Minimum Area Overlap Check (MOC)
Contact coverage



Minimum Width Check (MWC) - Pinching



Minimum Area Variability Check (MAVC)
Gate control



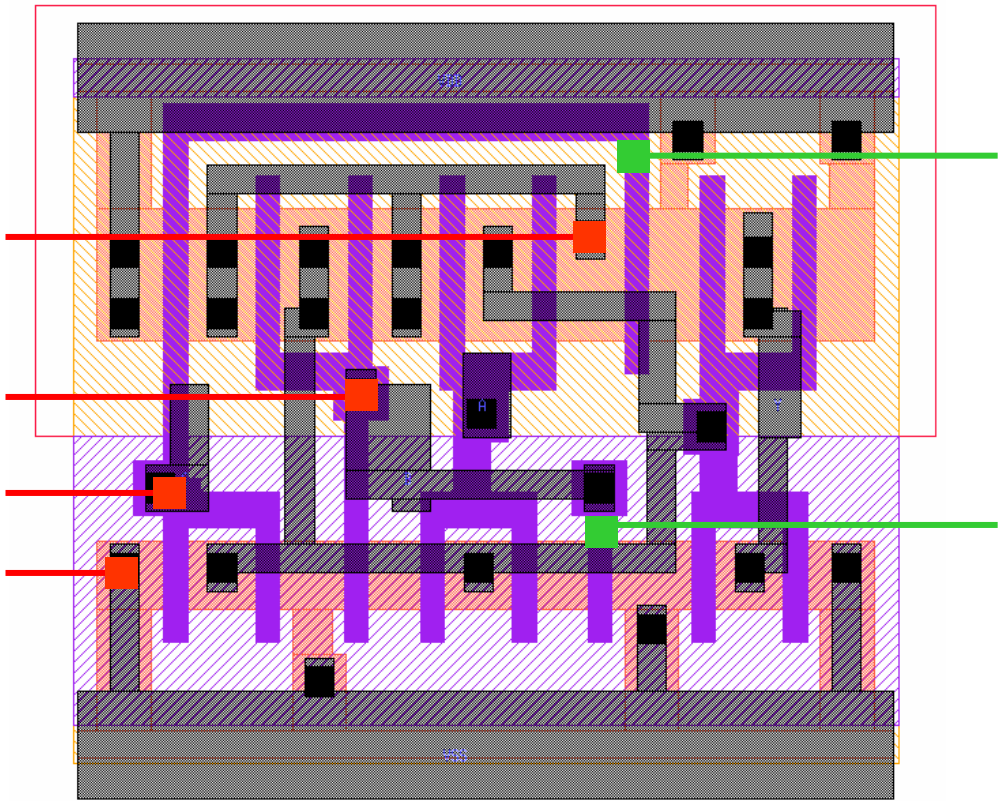
LFD-Guided Optimization Example

Layer	DVI
POLY	0.008
CONTACT	0.294
METAL1	0.004

Critical Errors: 6

4 -Non resolving contacts

2-Poly silicon pinching

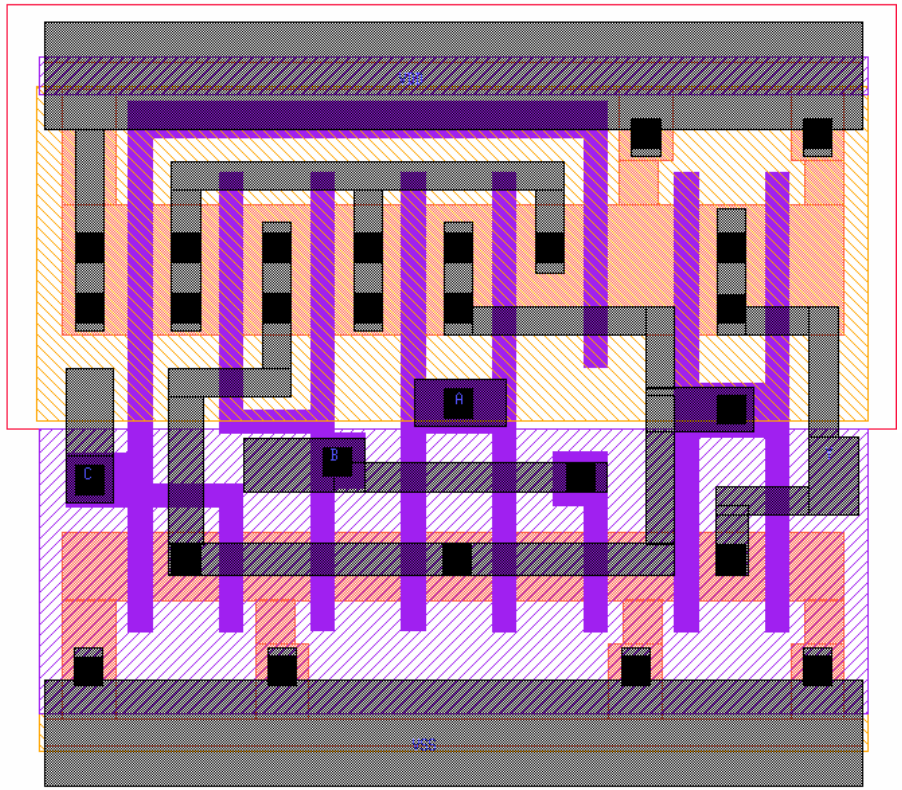


LFD Modifications

Layer	DVI
POLY	0.008
CONTACT	0.294
METAL1	0.004

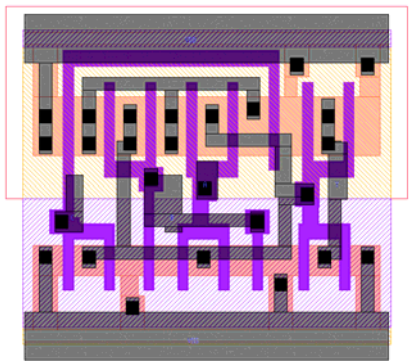
Critical Errors: None

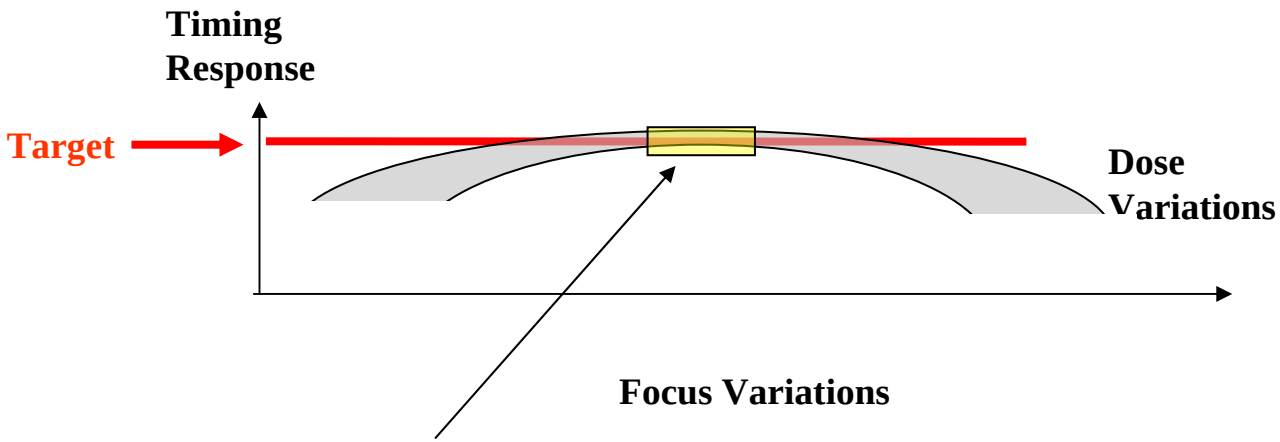
Layer	DVI
POLY	**0.007**
CONTACT	**0.000**
METAL1	**0.005**



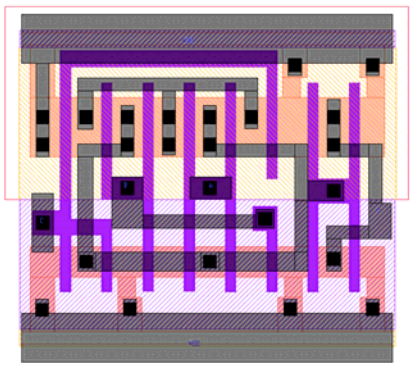
- Place contacts on grid
- Modify metal and poly

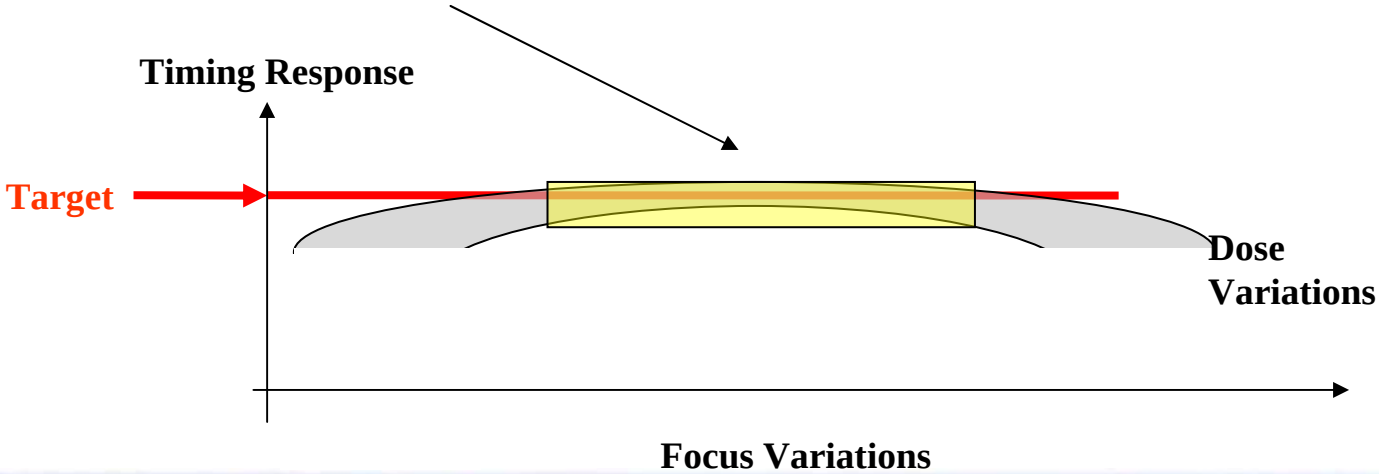
Parametric Benefit: Timing



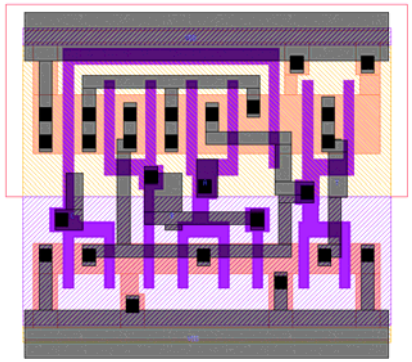


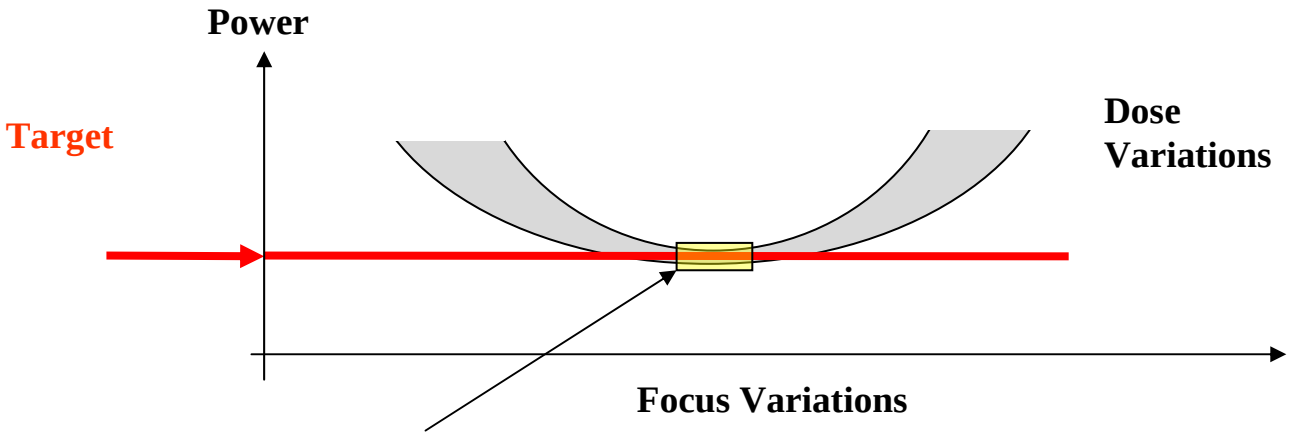
The optimized cell performs within spec even under larger process variability conditions





Parametric Benefit: Leakage





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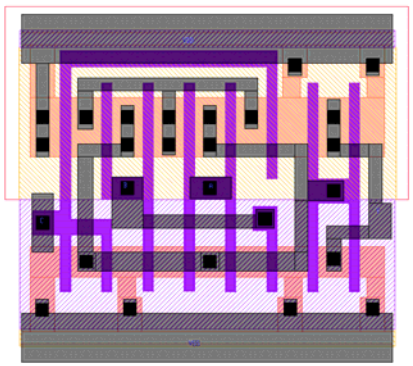
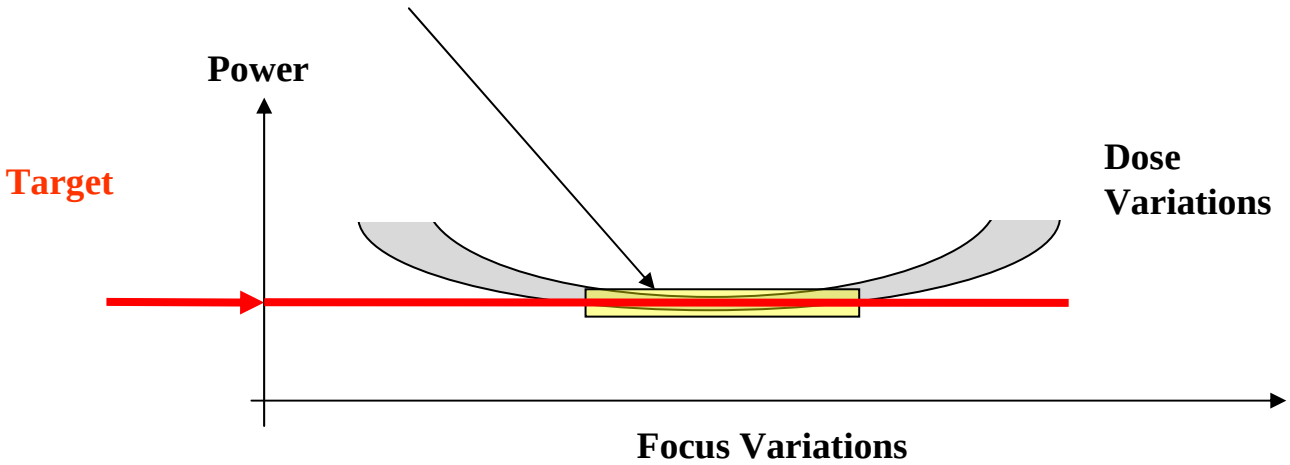
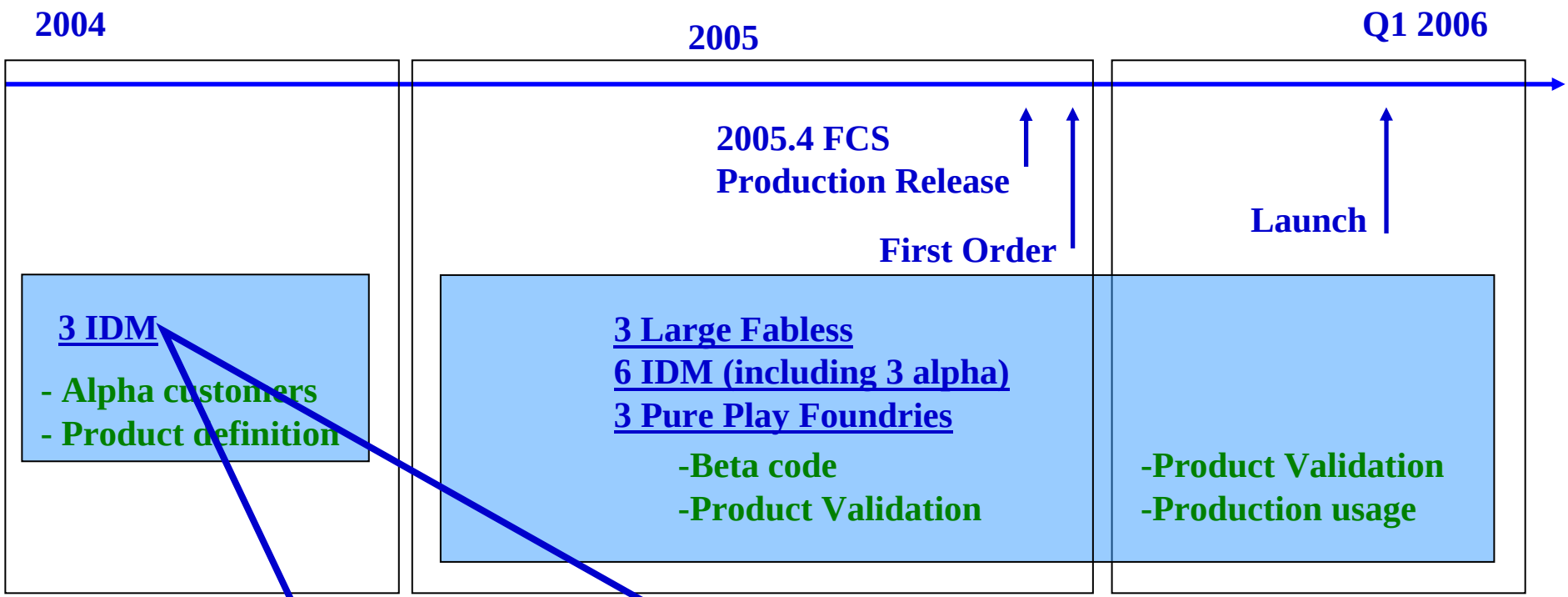


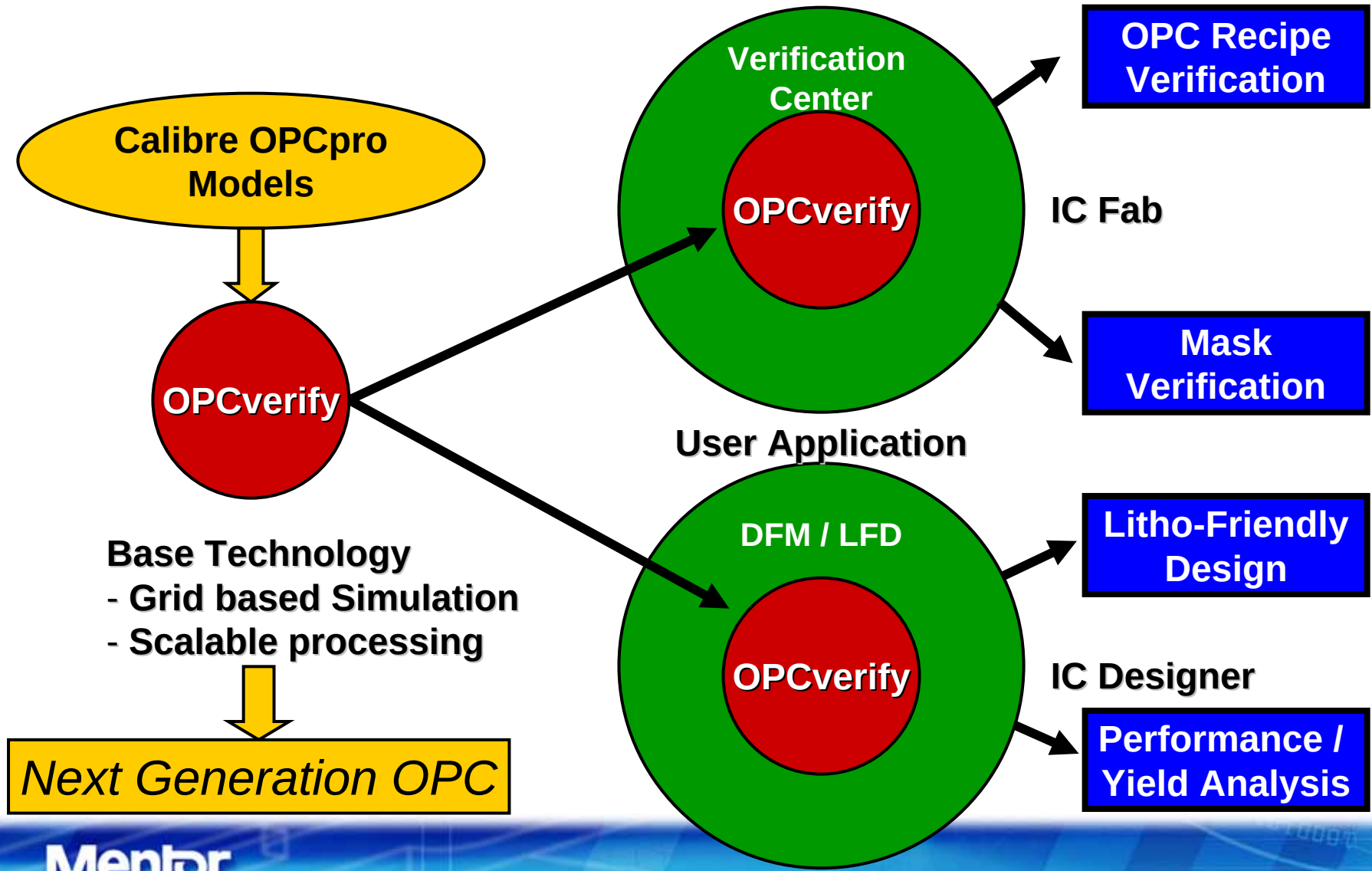


Engagement Status



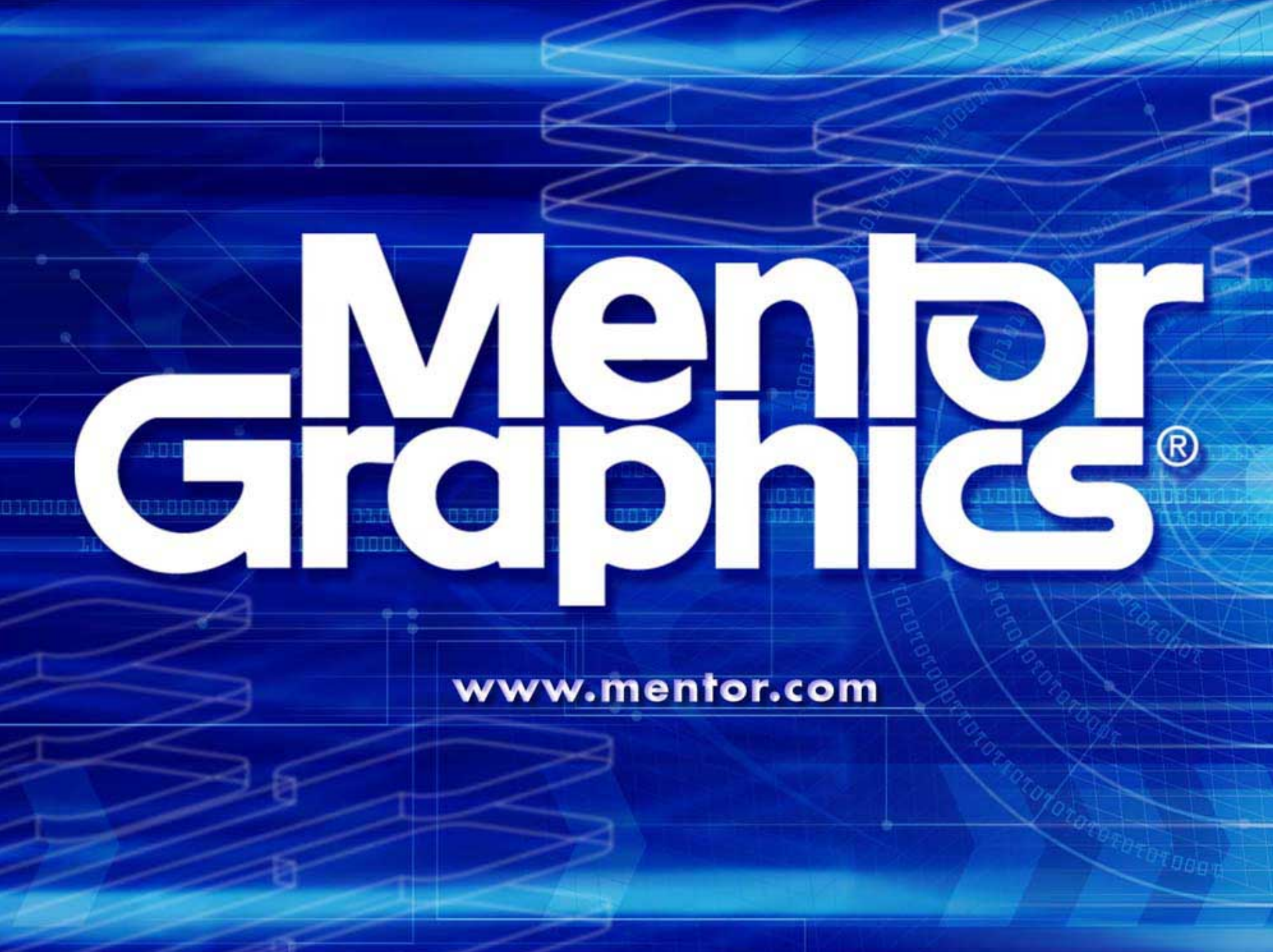
"The ability to deliver high yielding designs is critical in nanometer technology," **said Luigi Capodieci, Principal Member of Technical Staff at AMD.** ***"By adding Calibre LFD to our existing flow we can make layout modification tradeoffs at the earliest stages of design creation, and dramatically improve layout robustness across the process window."***

Leveragable Technology for Design and Production



Summary

- **Calibre LFD is for Layout Designers**
- **Integrated within current Design Environment**
  - **Fitting current Physical Verification (DRC) methodology**
- **Leverage production-proven modeling from OPC**
- **Giving the Layout designer the capability to verify/analyze that a layout will have acceptable Litho Yield**
  - **Systematic Yield (catastrophic failure check)**
  - **Parametric Yield**
  - **TTM as issues are found before fab**
- **Very successful engagements with teacher customers**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